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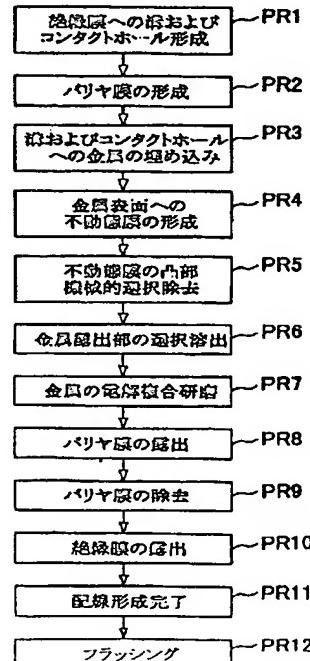
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(54)【発明の名称】 半導体装置の製造方法、研磨装置および研磨方法

(57)【要約】

【課題】多層配線構造を有する半導体装置の配線を構成するための金属膜の研磨による平坦化工程において、ディッシング、エロージョンの発生を抑制可能な、研磨方法、研磨装置および半導体装置の製造方法を提供する。

【解決手段】金属膜の表面に当該金属の電解反応を妨げる作用を発揮する不動態膜を形成する工程(PR4)と、配線用溝の埋め込みによって生じた金属膜の表面に存在する凸部上の不動膜を機械研磨によって選択的に除去し、金属膜の凸部を表面に露出させる工程(PR5)と、露出した金属膜の凸部を電解研磨によって除去し、配線用溝の埋め込みによって生じた金属膜の表面の凹凸を平坦化する工程(PR6)と、表面が平坦化された金属膜の絶縁膜上に存在する金属膜を電解研磨と機械研磨とを複合させた電解複合研磨によって除去し、前記配線を形成する工程(PR7)を有する。



【特許請求の範囲】

【請求項1】基板上に形成された絶縁膜に配線を形成するための配線用溝を形成する工程と、前記配線用溝を埋め込むように、前記絶縁膜上に金属膜を堆積させる工程と、前記絶縁膜上に堆積した金属膜の表面に当該金属膜の電解反応を妨げる作用を発揮する不動態膜を形成する工程と、前記金属膜に形成された不動態膜のうち、前記配線用溝の埋め込みによって生じた前記金属膜の表面に存在する凸部上の不動膜を機械研磨によって選択的に除去し、当該金属の凸部を表面に露出させる工程と、前記露出した金属膜の凸部を電解研磨によって除去し、前記配線用溝の埋め込みによって生じた前記金属膜の表面の凹凸を平坦化する工程とを有する半導体装置の製造方法。

【請求項2】前記表面が平坦化された金属膜の前記絶縁膜上に存在する余分な金属膜を電解研磨と機械研磨とを複合させた電解複合研磨によって除去し、前記配線を形成する工程をさらに有する請求項1に記載の半導体装置の製造方法。

【請求項3】前記電解複合研磨は、電解研磨と化学機械研磨とを複合させる請求項2に記載の半導体装置の製造方法。

【請求項4】前記配線用溝を形成した後に、前記絶縁膜上および前記溝内を覆うように前記金属膜の前記絶縁膜への拡散を防ぐための導電性材料からなるバリヤ膜を形成し、前記露出した金属膜の凸部を平坦化した後に、前記絶縁膜上に存在する余分な金属膜を前記電解複合研磨によって前記バリヤ膜が表面に露出するまで除去する工程と、

前記絶縁膜上に存在する余分なバリヤ膜を前記絶縁膜が表面に露出するまで前記電解複合研磨によって除去する工程とを有する請求項2に記載の半導体装置の製造方法。

【請求項5】導電性を有する研磨工具の研磨面と前記不動態膜との間に電解液を介在させ、前記金属膜およびバリヤ膜を陽極とし前記研磨工具を陰極として、前記金属膜およびバリヤ膜と前記研磨工具との間に電圧を印加し、

前記研磨工具を前記不動態膜の表面に相対的に移動させて、前記金属膜の凸部に形成された不動態膜を選択的に除去し、

前記選択的に除去された不動態膜から露出した前記金属膜の凸部を前記電解液の電解作用によって溶出させる請求項4に記載の半導体装置の製造方法。

【請求項6】前記研磨工具との間で電圧が印加された電極部材を前記金属膜およびバリヤ膜に接触または接近させて前記金属膜および前記バリヤ膜に通電し、

前記電極部材から前記前記金属膜および前記バリヤ膜を

経由して前記研磨工具に流れる電流をモニタリングし、当該電流値の大きさに基づいて前記金属膜およびバリヤ膜の研磨の進行を管理する請求項5に記載の半導体装置の製造方法。

【請求項7】前記研磨工具との間で電圧が印加された電極部材を前記金属膜およびバリヤ膜に接触または接近させて前記金属膜および前記バリヤ膜に通電し、前記電極部材と前記研磨工具との間に発生する電気抵抗の大きさをモニタリングし、当該電気抵抗値に基づいて前記金属膜およびバリヤ膜の研磨の進行を管理する請求項5に記載の半導体装置の製造方法。

【請求項8】前記研磨工具の研磨面と前記不動態膜との間に研磨砥粒を含む化学研磨剤を介在させて前記不動態膜を選択的に除去する請求項5に記載の半導体装置の製造方法。

【請求項9】前記金属膜と前記バリヤ膜とを構成する各材料に対してそれぞれ研磨レートの高い異なる化学研磨剤を用いて前記余分な金属膜とバリヤ膜とをそれぞれ除去する請求項5に記載の半導体装置の製造方法。

【請求項10】前記余分なバリヤ膜を除去する工程では、前記バリヤ膜と前記研磨工具との間に印加する電圧を、前記余分な金属膜を除去する工程での前記金属膜と前記研磨工具との間に印加する電圧よりも低くする請求項5に記載の半導体装置の製造方法。

【請求項11】前記配線用溝を形成する工程は、前記配線用溝の形成とともに、前記絶縁膜の下層に形成された不純物拡散層または配線と当該絶縁膜上に形成される配線とを接続するためのコンタクトホールを形成する工程を有し、

前記配線用溝に金属を埋め込む工程は、前記配線用溝とともに前記コンタクトホールに金属を埋め込む請求項2に記載の半導体装置の製造方法。

【請求項12】前記配線の形成材料には、銅を使用し、前記配線用溝およびコンタクトホールには電気メッキ法を用いて銅を埋め込む請求項11に記載の半導体装置の製造方法。

【請求項13】前記バリヤ膜の形成材料には、Ta、Ti、Ta_xNおよびTi_xNのいずれかを用いる請求項4に記載の半導体装置の製造方法。

【請求項14】前記不動態膜は、前記金属膜の表面を酸化させた酸化膜からなる請求項1に記載の半導体装置の製造方法。

【請求項15】前記金属膜の表面に酸化剤を供給して前記酸化膜を形成する請求項14に記載の半導体装置の製造方法。

【請求項16】前記不動態膜は、前記金属膜を構成する金属の電解反応を妨げる作用を発揮する材料からなる膜を前記金属膜の表面上に形成する請求項1に記載の半導体装置の製造方法。

【請求項17】前記不動態膜は、前記金属膜の表面に、

はう水膜、油膜、酸化防止膜、界面活性剤からなる膜、キレート剤からなる膜、および、シランカップリング剤からなる膜のいずれかを形成する請求項16に記載の半導体装置の製造方法。

【請求項18】前記不動態膜は、前記金属膜よりも、電気的抵抗が高く、かつ、機械的強度が低い請求項1に記載の半導体装置の製造方法。

【請求項19】研磨面を有し、導電性を有する研磨工具と、前記研磨工具を所定の回転軸を中心に回転させ、かつ、保持する研磨工具回転保持手段と、被研磨対象物を保持し所定の回転軸を中心に回転させる回転保持手段と、前記研磨工具を前記被研磨対象物に対向する方向の目標位置に移動位置決めする移動位置決め手段と、前記被研磨対象物の被研磨面と前記研磨工具の研磨面とを所定の平面に沿って相対移動させる相対移動手段と、前記被研磨対象物の被研磨面上に電解液を供給する電解液供給手段と、

前記被研磨対象物の被研磨面を陽極とし前記研磨工具を陰極として、前記被研磨面から前記電解液を通じて前記研磨工具に流れる電解電流を供給する電解電流供給手段とを有する研磨装置。

【請求項20】前記被研磨対象物の被研磨面に研磨砥粒を含む化学研磨剤を供給する研磨剤供給手段をさらに有する請求項19に記載の研磨装置。

【請求項21】前記電解電流供給手段は、前記被研磨対象物の被研磨面に接触可能または接近可能に配置され、前記被研磨対象物の被研磨面を陽極として当該被研磨面に通電する通電手段と、

前記通電手段と前記研磨工具との間に所定電位を印加する直流電源とを備える請求項1に記載の研磨装置。

【請求項22】前記直流電源は、所定周期のパルス状の電圧を出力する請求項21に記載の研磨装置。

【請求項23】前記研磨工具は、ホイール状の導電性部材からなり、当該部材の環状の一端面が研磨面を構成しており、

前記通電手段は、前記研磨工具の内側に当該研磨工具と離隔して設けられ、前記回転保持手段によって保持され、前記研磨工具とともに回転する導電性の電極板を備える請求項21に記載の研磨装置。

【請求項24】前記電極板は、前記被研磨対象物の被研磨面に對向する側に当該被研磨面をスクラップする面を有するスクラップ部材を備える請求項23に記載の研磨装置。

【請求項25】前記スクラップ部材は、前記電解液および研磨砥粒を含む化学研磨剤を吸収し、かつ通過させることができるものから形成されており、前記電極板側から供給される電解液および/または化学研磨剤を被研磨対象物の被研磨面に供給する請求項24に記載の研磨裝置。

置。

【請求項26】前記研磨工具は、前記回転保持手段に連結された導電性部材によって保持されており、前記回転する導電性部材に接触する通電ブラシを通じて通電される請求項21に記載の研磨装置。

【請求項27】前記電極部材は、前記被研磨対象物の被研磨面に形成された被電解金属に対して貴なる金属からなる請求項23に記載の研磨装置。

【請求項28】前記被研磨対象物の被研磨面から前記研磨工具に流れる電解電流の値を検出する電流検出手段をさらに備える請求項19に記載の研磨装置。

【請求項29】前記被研磨対象物の被研磨面を経由した前記電極部材と前記研磨工具との間の電気抵抗を検出する抵抗値検出手段を備える請求項23に記載の研磨装置。

【請求項30】前記電流検出手段の検出信号に基づいて、前記電解電流の値が一定となるように前記研磨工具と前記被研磨対象物との対向方向の位置を制御する制御手段をさらに有する請求項29に記載の研磨装置。

【請求項31】被研磨対象物の被研磨面の全面に回転しながら接触する研磨面を有する研磨工具を備え、前記被研磨対象物を前記研磨面に回転させながら接触させて平坦化研磨する研磨装置であって、前記研磨面上に電解液を供給する電解液供給手段を有し、

前記研磨面上に前記被研磨対象物の被研磨面に通電可能な陽極電極および陰極電極を備え、前記電解液による電解研磨と前記研磨面による機械研磨とを複合した電解複合研磨によって前記被研磨対象物の被研磨面を平坦化研磨する研磨装置。

【請求項32】前記研磨面に研磨砥粒を含む化学研磨剤を供給する研磨剤供給手段をさらに有し、

前記電解液による電解研磨と前記研磨面および前記研磨剤による化学機械研磨とを複合した電解複合研磨によって前記被研磨対象物の被研磨面を平坦化研磨する請求項31に記載の研磨装置。

【請求項33】導電性の研磨工具の研磨面と金属膜が少なくとも表面または内層に形成された被研磨対象物の表面とを電解液を介在させて押し付け、

前記研磨工具を陰極とし前記被研磨対象物の表面を陽極として、前記被研磨対象物の表面から前記研磨工具に前記電解液を通じて流れる電解電流を供給し、

前記研磨工具と前記被研磨対象物と共に回転させながら所定の平面に沿って相対移動させ、

前記電解液による電解研磨および前記研磨面による機械研磨を複合した電解複合研磨によって前記被研磨対象物に形成された金属膜を平坦化する研磨方法。

【請求項34】前記研磨面と前記被研磨対象物の表面との間に前記電解液とともに研磨砥粒を含む化学研磨剤を介在させ、前記電解液による電解研磨と前記研磨面およ

び前記研磨剤による化学機械研磨とを複合した電解複合研磨によって前記被研磨対象物に形成された金属膜を平坦化する請求項33に記載の研磨方法。

【請求項35】前記被研磨対象物には、異なる材料からなる複数の膜が積層されており、

前記各膜の材料の電気的特性の違いによって変化する前記電解液を通じて前記被研磨対象物の表面から前記研磨工具に流れる電解電流をモニタリングし、当該電解電流の大きさに基づいて研磨の進行を管理する請求項33に記載の研磨方法。

【請求項36】前記研磨工具と前記被研磨対象物の表面との間に、所定の周期のパルス状の電圧を印加して前記電解電流を供給する請求項33に記載の研磨方法。

【請求項37】電極部材を前記電解液が供給された前記被研磨対象物の表面に接近または当接させ、前記被研磨対象物の表面へ通電する請求項33に記載の研磨方法。

【請求項38】前記電極部材を前記研磨工具とともに回転させ、かつ、前記被研磨対象物に対して相対移動せながら前記被研磨対象物に形成された金属膜に通電する請求項37に記載の研磨方法。

【請求項39】前記被研磨対象物の表面を経由した前記電極部材と前記研磨工具との間の電気抵抗の大きさに基づいて、前記被研磨対象物の研磨の進行を管理する請求項37に記載の研磨方法。

【請求項40】前記研磨剤に含まれる研磨砥粒を正に帶電させる請求項34に記載の研磨方法。

【請求項41】被研磨対象物に形成された金属膜の表面に当該金属膜の電解反応を妨げる作用を發揮する不動態膜を形成する工程と、

導電性の研磨工具の研磨面と前記金属膜との間に電解液を介在させて当該研磨面と金属膜とを押し付け、かつ、前記研磨工具と前記金属膜と間に所定の電圧を印加する工程と、

前記研磨工具の研磨面と前記被研磨対象物の金属膜とを所定の平面に沿って相対移動させ、前記金属膜のうち前記研磨工具の研磨面に対して突出した凸部上の不動態膜を前記研磨工具の機械研磨によって選択的に除去する工程と、

前記不動態膜が除去されて表面に露出した金属膜の凸部を前記電解液による電解研磨作用によって除去して前記金属膜を平坦化する工程とを有する研磨方法。

【請求項42】前記研磨面と前記金属膜との間に前記電解液とともに研磨砥粒を含む化学研磨剤を介在させ、前記研磨面および前記研磨砥粒による化学機械研磨によって前記不動態膜を選択的に除去する請求項41に記載の研磨方法。

【請求項43】前記不動態膜は、前記金属膜の表面を酸化させた酸化膜からなる請求項41に記載の研磨方法。

【請求項44】前記不動態膜は、前記金属膜を構成する金属の電解反応を妨げる作用を發揮する材料からなる膜

を前記金属膜の表面上に形成する請求項41に記載の研磨方法。

【請求項45】前記不動態膜は、前記金属膜よりも、電気的抵抗が高く、かつ、機械的強度が低い請求項41に記載の研磨方法。

【請求項46】電極部材を前記金属膜の表面に接近または当接させ、前記金属膜へ通電する請求項41に記載の研磨方法。

【請求項47】前記電極部材と前記研磨工具との間の電気抵抗の大きさに基づいて研磨の進行を管理する請求項46に記載の研磨方法。

【請求項48】前記研磨剤に含まれる研磨砥粒を正に帶電させる請求項42に記載の研磨方法。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、たとえば、半導体装置の多層配線構造に伴う凹凸面を平坦化する研磨装置および研磨方法と多層配線構造をもつ半導体装置の製造方法に関する。

【0002】

【従来の技術】半導体装置の高集積化、小型化に伴い、配線の微細化、配線ピッチの縮小化、配線の多層化が進んでおり、半導体装置の製造プロセスにおける多層配線技術の重要性が増大している。一方、従来、多層配線構造の半導体装置の配線材料としてアルミニウム(A1)が多用されてきたが、最近の0.25μmルール以下のデザインルールにおいて、信号の伝搬遅延を抑制するために、配線材料をアルミニウム(A1)から銅(Cu)にえた配線プロセスの開発が盛んに行われている。Cuを配線に使用すると、低抵抗と高エレクトロマイグレーション耐性を両立できるというメリットがある。このCuを配線に使用したプロセスでは、たとえば、あらかじめ層間絶縁膜に形成した溝状の配線パターンに金属を埋め込み、CMP(Chemical Mechanical Polishing: 化学機械研磨)法によって余分な金属膜を除去して配線を形成する、ダマシン(damascene)法とよばれる配線プロセスが有力となっている。このダマシン法は、配線のエッチングが不要となり、さらに上の層間絶縁膜も自ずと平坦なものとなるので、工程を簡略化できるという特徴を有する。さらに、層間絶縁膜に配線だけでなく、コンタクトホールも溝として開け、配線とコンタクトホールを同時に金属で埋め込むデュアルダマシン(dual damascene)法では、さらに大幅な配線工程の削減が可能となる。

【0003】ここで、上記のデュアルダマシン法による配線形成プロセスの一例について図32～図37を参照して説明する。なお、配線材料としてCuを用いた場合について説明する。まず、図32に示すように、たとえば、図示しない不純物拡散領域が適宜形成されているシリコン等の半導体からなる基板301上に、たとえば、

シリコン酸化膜からなる層間絶縁膜302を、たとえば、減圧CVD(Chemical Vapour Deposition)法により形成する。次いで、図33に示すように、基板301の不純物拡散領域に通じるコンタクトホール303および基板301の不純物拡散領域と電気的に接続される所定パターンの配線が形成される溝304を公知のフォトリソグラフィ技術およびエッティング技術を用いて形成する。次いで、図34に示すように、バリヤ膜305を層間絶縁膜302の表面およびコンタクトホール303、溝304内に形成する。このバリヤ膜305は、たとえば、Ta、Ti、TaN、TiN等の材料を公知のスパッタ法により形成する。バリヤ膜305は、配線を構成する材料が層間絶縁膜302中に拡散するのを防止するために設けられる。特に、配線材料がCuで層間絶縁膜302がシリコン酸化膜のような場合には、Cuはシリコン酸化膜への拡散係数が大きく、酸化されやすいため、これを防止する。

【0004】次いで、図35に示すように、バリヤ膜305上に、シードCu膜306を公知のスパッタ法により所定の膜厚で形成し、次いで、図36に示すように、コンタクトホール303および溝304をCuで埋め込むように、Cu膜307を形成する。Cu膜307は、たとえば、メッキ法、CVD法、スパッタ法等によって形成する。次いで、図37に示すように、層間絶縁膜302上の余分なCu膜307およびバリヤ膜305をCMP法によって除去し、平坦化する。これによって、配線308およびコンタクト309が形成される。上記したプロセスを配線308上で繰り返し行うことにより、多層配線を形成することができる。

【0005】

【発明が解決しようとする課題】ところで、上記したデュアルダマシン法を用いた多層配線形成プロセスでは、余分なCu膜307およびバリヤ膜305をCMP法によって除去する工程において、層間絶縁膜302とCu膜307およびバリヤ膜305との除去性能が異なることから、配線308にディッシング、エロージョン(シンニング)、リセス等が発生しやすいという不利益が存在した。ディッシングは、図38に示すように、たとえば、0.18μmルールのデザインルールにおいて、たとえば、100μm程度のような幅の広い配線308が存在した場合に、当該配線の中央部が過剰に除去されへこんでしまう現象であり、このディッシングが発生すると配線308の断面積が不足するため、配線抵抗値不良等の原因となる。このディッシングは、配線材料に比較的軟質の銅やアルミニウムを用いた場合に発生しやすい。エロージョンは、図39に示すように、たとえば、3000μmの範囲に1.0μmの幅の配線が50パーセントの密度で形成されているようなパターン密度の高い部分が過剰に除去されてしまう現象であり、エロージョンが発生すると配線の断面積が不足するため、配線抵

抗値不良等の原因となる。リセスは、図40に示すように、層間絶縁膜302と配線308との境界で配線308が低くなり段差ができてしまう現象であり、この場合にも配線の断面積が不足するため、配線抵抗値不良等の原因となる。さらに、余分なCu膜307およびバリヤ膜305をCMP法によって除去する工程では、Cu膜307およびバリヤ膜305を効率的に除去する必要があり、単位時間当たりの除去量である研磨レートは、たとえば、500nm/min以上となるように要求されている。この研磨レートを稼ぐためにはウェーハに対する加工圧力を大きくする必要があり、加工圧力を大きくすると、図41に示すように、配線表面にスクラッチSCやケミカルダメージCDが発生しやすくなり、特に、軟質のCuやアルミニウムでは発生しやすい。このため、配線のオープン、ショート、配線抵抗値不良等の不具合の原因となり、また、加工圧力を大きくすると、上記のディッシング、エロージョン、リセスの発生量も大きくなるという不利益が存在した。

【0006】本発明は、上記した問題に鑑みてなされたものであって、たとえば、多層配線構造を有する半導体装置の配線等の金属膜を研磨によって平坦化する際に、初期凹凸を容易に平坦化でき、かつ余分な金属膜の除去効率に優れ、ディッシング、エロージョン等の金属膜の過剰な除去の発生を抑制可能な研磨装置および研磨方法、半導体装置の製造方法を提供する。

【0007】

【課題を解決するための手段】本発明の研磨装置は、研磨面を有し、導電性を有する研磨工具と、前記研磨工具を所定の回転軸を中心に回転させ、かつ、保持する研磨工具回転保持手段と、被研磨対象物を保持し所定の回転軸を中心に回転させる回転保持手段と、前記研磨工具を前記被研磨対象物に対向する方向の目標位置に移動位置決めする移動位置決め手段と、前記被研磨対象物の被研磨面と前記研磨工具の研磨面とを所定の平面に沿って相対移動させる相対移動手段と、前記被研磨対象物の被研磨面上に電解液を供給する電解液供給手段と、前記被研磨対象物の被研磨面を陽極とし前記研磨工具を陰極として、前記被研磨面から前記電解液を通じて前記研磨工具に流れる電解電流を供給する電解電流供給手段とを有する。

【0008】また、本発明の研磨装置は、被研磨対象物の被研磨面の全面に回転しながら接触する研磨面を有する研磨工具を備え、前記被研磨対象物を前記研磨面に回転させながら接触させて平坦化研磨する研磨装置であって、前記研磨面上に電解液を供給する電解液供給手段を有し、前記研磨面上に前記被研磨対象物の被研磨面に通電可能な陽極電極および陰極電極を備え、前記電解液による電解研磨と前記研磨面による機械研磨とを複合した電解複合研磨によって前記被研磨対象物の被研磨面を平坦化研磨する。

【0009】本発明の研磨方法は、導電性の研磨工具の研磨面と金属膜が少なくとも表面または内層に形成された被研磨対象物の表面とを電解液を介在させて押し付け、前記研磨工具を陰極とし前記被研磨対象物の表面を陽極として、前記被研磨対象物の表面から前記研磨工具に前記電解液を通じて流れる電解電流を供給し、前記研磨工具と前記被研磨対象物とを共に回転させながら所定の平面に沿って相対移動させ、前記電解液による電解研磨および前記研磨面による機械研磨を複合した電解複合研磨によって前記被研磨対象物に形成された金属膜を平坦化する。

【0010】また、本発明の研磨方法は、被研磨対象物に形成された金属膜の表面に当該金属膜の電解反応を妨げる作用を発揮する不動態膜を形成する工程と、導電性の研磨工具の研磨面と前記金属膜との間に電解液を介在させて当該研磨面と金属膜とを押し付け、かつ、前記研磨工具と前記金属膜と間に所定の電圧を印加する工程と、前記研磨工具の研磨面と前記被研磨対象物の金属膜とを所定の平面に沿って相対移動させ、前記金属膜のうち前記研磨工具の研磨面に対して突出した凸部上の不動態膜を前記研磨工具の機械研磨によって選択的に除去する工程と、前記不動態膜が除去されて表面に露出した金属膜の凸部を前記電解液による電解研磨作用によって除去して前記金属膜を平坦化する工程とを有する。

【0011】本発明の半導体装置の製造方法は、基板上に形成された絶縁膜に配線を形成するための配線用溝を形成する工程と、前記配線用溝を埋め込むように、前記絶縁膜上に金属膜を堆積させる工程と、前記絶縁膜上に堆積した金属膜の表面に当該金属膜の電解反応を妨げる作用を発揮する不動態膜を形成する工程と、前記金属膜に形成された不動態膜のうち、前記配線用溝の埋め込みによって生じた前記金属膜の表面に存在する凸部上の不動膜を機械研磨によって選択的に除去し、当該金属の凸部を表面に露出させる工程と、前記露出した金属膜の凸部を電解研磨によって除去し、前記配線用溝の埋め込みによって生じた前記金属膜の表面の凹凸を平坦化する工程とを有する。

【0012】また、本発明の半導体装置の製造方法は、前記表面が平坦化された金属膜の前記絶縁膜上に存在する余分な金属膜を電解研磨と機械研磨とを複合させた電解複合研磨によって除去し、前記配線を形成する工程をさらに有する。

【0013】本発明の半導体装置の製造方法では、表面に凹凸がある金属膜に不動態膜を形成し、不動態膜を機械的に除去することで、金属膜の凸部が表面に露出する。この金属膜の凸部は残った不動態膜をマスクとして電解液による電解作用によって選択的に溶出する。この結果、金属膜の初期凹凸が平坦化される。また、初期凹凸が平坦化された金属膜は、電解複合研磨によって高能率に除去され、たとえば、配線を形成する際に絶縁膜上

に存在する余分な金属膜は高能率に除去される。余分な金属膜が除去されて絶縁膜が露出すると、自動的にその部分の電解作用が停止し、絶縁膜に形成された配線用溝に埋め込まれた金属膜が過剰に除去されない。

【0014】

【発明の実施の形態】以下、本発明の実施の形態について図面を参照して説明する。

研磨装置の構成

図1は、本発明の一実施形態に係る研磨装置の構成を示す図である。図2は図1に示す研磨装置の加工ヘッド部の要部拡大図である。図1に示す研磨装置1は、加工ヘッド部2と、電解電源61と、研磨装置1全体を制御する機能を有するコントローラ55と、スラリー供給装置71と、電解液供給装置81とを備えている。なお、図示しないが、研磨装置1は、クリーンルーム内に設置され、当該クリーンルーム内には被研磨対象物としてのウェーハを収容したウェーハカセットを搬出入する搬出入口が設けられている。さらに、この搬出入口を通してクリーンルーム内に搬入されたウェーハカセットと研磨装置1との間でウェーハの受け渡しを行うウェーハ搬送ロボットが搬出入口と研磨装置1との間に設置される。

【0015】加工ヘッド部2は、研磨工具3を保持し回転させ、研磨工具3を保持する研磨工具保持部11と、研磨工具保持部11をZ軸方向の目標位置に位置決めするZ軸位置決め機構部31と、被研磨対象物としてのウェーハWを保持し回転させX軸方向に移動するX軸移動機構部41とを備える。なお、研磨工具保持部11が本発明の研磨工具回転保持手段の一具体例に対応しており、X軸移動機構部41が本発明の回転保持手段および相対移動手段の一具体例に対応しており、Z軸位置決め機構部31は本発明の移動位置決め手段の一具体例に対応している。

【0016】Z軸位置決め機構部31は、図示しないコラムに固定されたZ軸サーボモータ18と、保持装置12および主軸モータ13に連結され、Z軸サーボモータ18に接続されたポールネジ軸18aに螺合するネジ部が形成されたZ軸スライダ16と、Z軸スライダ16をZ軸方向に移動自在に保持する図示しないコラムに設置されたガイドレール17とを有する。

【0017】Z軸サーボモータ18は、Z軸サーボモータ18に接続されたZ軸ドライバ52から駆動電流が供給されて回転駆動される。ポールネジ軸18aは、Z軸方向方向に沿って設けられ、一端がZ軸サーボモータ18に接続され、他端は、上記の図示しないコラムに設けられた保持部材によって回転自在に保持されている。これにより、Z軸位置決め機構部31は、Z軸サーボモータ18の駆動によって、研磨工具保持部11に保持された研磨工具3をZ軸方向の任意の位置に移動位置決めする。Z軸位置決め機構部31の位置決め精度は、たとえ

ば、分解能0.1μm程度としている。

【0018】X軸移動機構41は、ウェハWをチャギングするウェハテーブル42と、ウェハテーブル42を回転自在に保持する保持装置45と、ウェハテーブル42を回転させる駆動力を供給する駆動モータ44と、駆動モータ44と保持装置45の回転軸とを連結するベルト46と、保持装置45に設けられた加工パン47と、駆動モータ44および保持装置45が設置されたX軸スライダ48と、図示しない架台に基台されたX軸サーボモータ49と、X軸サーボモータ49に接続されたボールネジ軸49aと、X軸スライダ48に連結されボールネジ軸49aに螺合するネジ部が形成された可動部材49bとを有する。

【0019】ウェハテーブル42は、たとえば、真空吸着手段によってウェハWを吸着する。加工パン47は、使用済の電解液や、スラリー等の液体を回収するために設けられている。駆動モータ44は、テーブルドライバ53から駆動電流が供給されることによって駆動され、この駆動電流を制御することでウェハテーブル42を所定の回転数で回転させることができる。X軸サーボモータ49は、X軸サーボモータ49に接続されたX軸ドライバ54から供給される駆動電流によって回転駆動し、X軸スライダ48がボールネジ軸49aおよび可動部材49bを介してX軸方向に駆動する。このとき、X軸サーボモータ49に供給する駆動電流を制御することによって、ウェハテーブル42のX軸方向の速度制御が可能となる。

【0020】図2は、研磨工具保持部11の内部構造の一例を示す図である。研磨工具保持部11は、研磨工具3と、研磨工具3を保持するフランジ部材4と、フランジ部材4を回転自在に保持する保持装置12と、保持装置12に保持された主軸12aと接続され当該主軸12aを回転させる主軸モータ13と、主軸モータ13上に設けられたシリング装置14とを備える。

【0021】主軸モータ13は、たとえば、ダイレクトドライブモータからなり、このダイレクトドライブモータの図示しないロータは、保持装置12に保持された主軸12aに連結されている。また、主軸モータ13は中心部にシリング装置14のピストンロッド14bが挿入される貫通孔を有している。主軸モータ13は、主軸ドライバ51から供給される駆動電流によって駆動される。

【0022】保持装置12は、たとえば、エアベアリングを備えており、このエアベアリングで主軸12aを回転自在に保持している。保持装置12の主軸12aも中心部にシリング装置14のピストンロッド14bが挿入される貫通孔を有している。

【0023】フランジ部材4は、金属材料から形成されており、保持装置12の主軸12aに連結され、底部に開口部4aを備え、下端面4bに研磨工具3が固定され

ている。フランジ部材4の上端面4c側は保持装置12に保持された主軸12aに連結されており、主軸12aの回転によってフランジ部材4も回転する。フランジ部材4の上端面4cは、主軸モータ13および保持装置12の側面に設けられた導電性の通電部材28に固定された通電ブラシ27と接触しており、通電ブラシ27とフランジ部材4とは電気的に接続されている。

【0024】シリング装置14は、主軸モータ13のケース上に固定されており、ピストン14aを内蔵しており、ピストン14aは、たとえば、シリング装置14内に供給される空気圧によって矢印A1およびA2のいずれかの向きに駆動される。このピストン14aには、ピストンロッド14bが連結されており、ピストンロッド14bは、主軸モータ13および保持装置12の中心を通って、フランジ部材4の開口部4aから突き出ている。ピストンロッド14bの先端には、押圧部材21が連結されており、この押圧部材21はピストンロッド14bに対して所定の範囲で姿勢変更が可能な連結機構によって連結されている。押圧部材21は、対向する位置に配置された絶縁板22の開口22aの周縁部に当接可能となっており、ピストンロッド14bの矢印A2方向への駆動によって絶縁板22を押圧する。

【0025】シリング装置14のピストンロッド14bの中心部には、貫通孔が形成されており、貫通孔内に通電軸20が挿入され、ピストンロッド14bに対して固定されている。通電軸20は、導電性材料から形成されており、上端側はシリング装置14のピストン14aを貫通してシリング装置14上に設けられたロータリジョイント15まで伸びており、下端側は、ピストンロッド14bおよび押圧部材21を貫通して電極板23まで伸びており、電極板23に接続されている。

【0026】通電軸20は、中心部に貫通孔が形成されており、この貫通孔が化学研磨剤(スラリー)および電解液をウェハW上に供給する供給ノズルとなっている。また、通電軸20は、ロータリジョイント15と、電極板23とを電気的に接続する役割を果たしている。

【0027】通電軸20の上端部に接続されたロータリジョイント15は、電解電極61のプラス極と電気的に接続されており、このロータリジョイント15は通電軸20が回転しても通電軸20への通電を維持する。すなわち、通電軸20は回転してもロータリジョイント15によって電解電極61からプラスの電位が印加される。

【0028】通電軸20の下端部に接続された電極板23は、金属材料からなり、特に、ウェハWに形成される金属膜より貴なる金属で形成されている。電極板23は、上面側が絶縁板22に保持されており、電極板23の外周部は絶縁板22に嵌合しており、下面側にはスクラブ部材24が貼着されている。

【0029】ここで、図3(a)は電極板23の構造の一例を示す下面図であり、図3(b)は電極板23と、

通電軸20、スクラップ部材24および絶縁部材4との位置関係を示す断面図である。図3(a)に示すように、電極板23の中央部には円形の開口部23aが設けられており、この開口部23aを中心に電極板23の半径方向に放射状に伸びる複数の溝部23bが形成されている。また、図3(b)に示すように、電極板23の開口部23aには、通電軸20の下端部が嵌合固定されている。このような構成とすることで、通電軸20の中心部に形成された供給ノズル20aを通じて供給されるスラリーおよび電解液が溝部23bを通じてスクラップ部材24の全面に拡散するようになっている。すなわち、電極板23と、通電軸20、スクラップ部材24および絶縁部材4が回転しながら、スラリーおよび電解液が通電軸20の中心部に形成された供給ノズル20aを通じてスクラップ部材24の上側面に供給されると、スクラップ部材24の上側面全体にスラリーおよび電解液が広がる。なお、スクラップ部材24および通電軸20の供給ノズル20aが本発明の研磨剤供給手段および電解液供給手段の一具体例に対応している。また、電極板23、通電軸20およびロータリジョイント15が本発明の通電手段の一具体例に対応している。

【0030】電極板23の下面に貼着されたスクラップ部材24は、電解液およびスラリーを吸収し、これらを上側面から下側面に通過させることができる材料から形成されている。また、このスクラップ部材24は、ウェーハWに向向する面がウェーハWに接触してウェーハWをスクラップする面となっており、ウェーハW表面にスクラッチ等を発生させないように、たとえば、柔らかいブラシ状の材料、スポンジ状の材料、多孔質の材料等から形成される。たとえば、ウレタン樹脂、メラミン樹脂、エポキシ樹脂、ポリビニルアセタール(PVA)などの樹脂からなる多孔質体が挙げられる。

【0031】絶縁板22は、たとえば、セラミクス等の絶縁材料から形成されており、この絶縁板22は複数の棒状の連結部材26によって保持装置12の主軸12aに連結されている。連結部材26は、絶縁板22の中心軸から所定の半径位置に等間隔に配置されており、保持装置12の主軸12aに対して移動自在に保持されている。このため、絶縁板22は主軸12aの軸方向に移動可能である。また、絶縁板22と主軸12aとの間にには、各連結部材26に対応して、たとえば、コイルスプリングからなる弾性部材25で接続されている。

【0032】絶縁板22を保持装置12の主軸12aに対して移動自在にし、絶縁板22と主軸12aとを弾性部材25で連結する構成とすることにより、シリンダ装置14に高圧エアを供給してピストンロッド14bを矢印A2の向きに下降させると、押圧部材21が弾性部材25の復元力に逆らって絶縁板22を下方に押し下げ、これとともにスクラップ部材24も下降する。この状態からシリンダ装置14への高圧エアの供給を停止すると、

弾性部材25の復元力によって、絶縁板22は上昇し、これとともにスクラップ部材24も上昇する。

【0033】研磨工具3は、フランジ部材4の環状の下端面4bに固着されている。この研磨工具3は、ホール状に形成されており、下端面に環状の研磨面3aを備えている。研磨工具3は、導電性を有しており、好ましくは、比較的軟質性の材料で形成する。たとえば、バイオンドマトリクス(結合剤)自体が導電性を持つカーボンや、あるいは、焼結銅、メタルコンパウンド等の導電性材料を含有するウレタン樹脂、メラミン樹脂、エポキシ樹脂、ポリビニルアセタール(PVA)などの樹脂からなる多孔質体から形成することができる。研磨工具3は、導電性を有するフランジ部材4に直接接続され、フランジ部材4に接触する通電ブラシ27から通電される。すなわち、主軸モータ13および保持装置12の側面に設けられた導電性の通電部材28は、電解電源61のマイナス極と電気的に接続され、通電部材28に設けられた通電ブラシ27はフランジ部材4の上端面4cに接触しており、これにより、研磨工具3は電解電源61と通電部材28、通電ブラシ27およびフランジ部材4を介して電気的に接続されている。

【0034】研磨工具3は、たとえば、図4に示すように、研磨面3aは中心軸に対して微小角度で傾斜している。また、保持部材12の主軸12aもウェーハWの正面に対して研磨面3aの傾斜と同様に傾斜している。たとえば、保持部材12のZ軸スライダ16への取り付け姿勢を調整することで主軸12aの微小な傾斜をつくり出すことができる。このように、研磨工具3の中心軸がウェーハWの正面に対して微小角度で傾斜していることにより、研磨工具3の研磨面3aを所定の加工圧力FでウェーハWに押し付けた際に、研磨面3aのウェーハWに対する実効的な作用領域Sが図4に示すように、研磨工具3の半径方向に伸びる直線状の領域となる。このため、ウェーハWを研磨工具3に対してX軸方向に移動させて研磨下降を行う際に、図5(a)の状態から図5(b)に移動する間、実効的な作用領域Sの面積は略一定となる。本実施形態に係る研磨装置1では、研磨工具3の研磨面3aの一部を部分的にウェーハWの表面に作用させ、実効的な作用領域SをウェーハWの表面に均一に走査させてウェーハWの全面を均一に研磨する。

【0035】電解電源61は、上記したロータリジョイント15と通電ブラシ12との間に所定の電圧を印加する装置である。ロータリジョイント15と通電ブラシ12との間に電圧を印加することによって、研磨工具3とスクラップ部材24との間には電位差が発生する。電解電源61には、常に一定の電圧を出力する定電圧電源ではなく、好ましくは、電圧を一定周期でパルス状に出力する、たとえば、スイッチング・レギュレータ回路を内蔵した直流電源を使用する。具体的には、パルス状の電圧を一定周期で出力し、パルス幅を適宜変更可能な電源を

使用する。一例としては、出力電圧がDC 150V、最大出力電流が2~3A、パルス幅が1, 2, 5, 10, 20, 50μsのいずれかに変更可能なものを使用した。上記のような幅が短いパルス状の電圧出力をするのは、1パルス当たりの電解溶出量を非常に小さくするためである。すなわち、ウェーハWの表面に形成された金属膜の凹凸や接触した場合などにみられる極間距離の急変による放電、気泡やパーティクルなどが介在した場合における電気抵抗の急変によるスパーク放電など、金属膜の突発的なクレータ状の巨大溶出を防止、あるいは、できる限り抑制する小さなものの連続にするために有効である。また、出力電流に比して出力電圧が比較的高いため、極間距離の設定にある程度のマージンを設定する事ができる。すなわち、極間距離が多少変わっても出力電圧が高いため電流値変化は小さい。

【0036】電解電源61には、本発明の電流検出手段としての電流計62を備えており、この電流計62は、電解電源61に流れる電解電流をモニタするために設けられており、モニタした電流値信号62sをコントーラ55に出力する。また、電解電源61は、本発明の抵抗値検出手段としての抵抗計63を備えており、この抵抗計63は電解電源61に流れる電流に基づいて、ウェーハWの表面を経由した研磨工具3と電極板23との間の電気抵抗をモニタリングするために設けられており、モニタリングした電気抵抗値信号63sをコントーラ55に出力する。

【0037】スラリー供給装置71は、スラリーを上記の通電軸20の供給ノズル20aに供給する。スラリーとしては、金属膜の研磨用として、たとえば、過酸化水素、硝酸鉄、ヨウ素酸カリウム等をベースとした酸化力のある水溶液に酸化アルミニウム（アルミナ）、酸化セリウム、シリカ、酸化ゲルマニウム等を研磨砥粒として含有させたものを使用する。また、研磨砥粒は、分散性を良くしてコロイド状態を保持するために予め正に帯電させておく。

【0038】電解液供給装置81は、電解液E-Lを加工ヘッド部11に供給する。電解液E-Lは、溶媒とイオン的に分離した溶質とからなる溶液である。この電解液として、たとえば、硝酸塩あるいは塩化物系に還元剤を調整した水溶液を使用することができる。

【0039】コントーラ55は、研磨装置1の全体を制御する機能を有し、具体的には、主軸ドライバ51に対して制御信号51sを出力して研磨工具3の回転数を制御し、Z軸ドライバ52に対して制御信号52sを出力して研磨工具3のZ軸方向の位置決め制御を行い、テーブルドライバ53に対して制御信号53sを出力してウェーハWの回転数を制御し、X軸ドライバ54に対して制御信号54sを出力して、ウェーハWのX軸方向の速度制御を行う。また、コントーラ55は、電解液供給装置81およびスラリー供給装置71の動作を制御

し、加工ヘッド部2への電解液E-Lおよびスラリー-SLの供給動作を制御する。

【0040】また、コントーラ55は、電解電源61の出力電圧、出力パルスの周波数、出力パルスの幅等を制御可能となっている。また、コントーラ55には、電解電源61の電流計62および抵抗計63からの電流値信号62sおよび電気抵抗値信号63sが入力される。コントーラ55は、これら電流値信号62sおよび電気抵抗値信号63sに基づいて、研磨装置1の動作を制御可能となっている。具体的には、電流値信号62sから得られた電解電流が一定となるように、電流値信号62sをフィードバック信号としてZ軸サーボモータ18の制御したり、電流値信号62sまたは電気抵抗値信号63sで特定される電流値、電気抵抗値の値に基づいて、研磨加工を停止させるように研磨装置1の動作を制御する。

【0041】コントーラ55に接続されたコントロールパネル56は、オペレータが各種のデータを入力したり、たとえば、モニタリングした電流値信号62sおよび電気抵抗値信号63sを表示したりする。

【0042】次に、上記した研磨装置1による研磨動作をウェーハW表面に形成された金属膜を研磨する場合を例に説明する。なお、ウェーハWの表面には、たとえば、銅からなる金属膜が形成されている場合について説明する。まず、ウェーハテーブル45にウェーハWをチャッキングし、ウェーハテーブル45を駆動して所定の回転数でウェーハWを回転させる。また、ウェーハテーブル45をX軸方向に移動して、フランジ部4に取り付けられた研磨工具3をウェーハWの上方の所定位置に位置させ、研磨工具3を所定の回転数で回転させる。研磨工具3を回転させると、フランジ部4に連結された絶縁板22、電極板23およびスクラップ部材24も回転駆動される。また、スクラップ部材24を押圧している押圧部材21、ピストンロッド14b、ピストン14a、通電軸20も同時に回転する。

【0043】この状態から、スラリー供給装置71および電解液供給装置81からそれぞれスラリー-SLおよび電解液E-Lを通電軸20内の供給ノズル20aに供給すると、スクラップ部材24の全面からスラリー-SLおよび電解液E-Lが供給される。研磨工具3をZ軸方向に下降させて研磨工具3の研磨面3aをウェーハWの表面に接触させ、所定の加工圧力を押圧させる。また、電解電源61を起動させて、通電ブラシ27を通じて研磨工具3にマイナスの電位を印加し、ロークリジョント15を通じてスクラップ部材24にプラスの電位を印加する。

【0044】さらに、シリンダ装置14に高圧エアを供給して、図1の矢印A2の方向にピストンロッド14bを下降させ、スクラップ部材24の下面をウェーハWに接触あるいは接近する位置まで移動させる。この状態からウェーハテーブル45をX軸方向に所定の速度パターン

で移動させ、ウェーハWの全面を一様に研磨加工する。【0045】ここで、図6は、研磨装置1において研磨工具3をZ軸方向に下降させ、ウェーハWの表面に接触させた状態を示す概略図であり、図7は図6の円C内の拡大図であり、図8は図7の円D内の拡大図である。図7に示すように、スクラップ部材24はウェーハWに形成された金属膜MTに、ウェーハW上に供給された電解液ELを介して、または、直接接触することにより陽極として通電し、研磨工具3もウェーハWに形成された金属膜MTに、ウェーハW上に供給された電解液ELを介して、または、直接接触することにより陰極として通電する。なお、図7に示すように、金属膜MTとスクラップ部材24との間には、ギャップδbが存在している。さらに、図8に示すように、金属膜MTと研磨工具3の研磨面3aとの間にはギャップδwが存在している。図7に示すように、絶縁板4は、研磨工具3とスクラップ部材24(電極板23)との間に介在しているが、絶縁板4の抵抗R0は非常に大きく、したがって、スクラップ部材24から絶縁板4を介して研磨工具3に流れる電流i1はほぼ零であり、スクラップ部材24から絶縁板4を介して研磨工具3には電流が流れない。

【0046】このため、スクラップ部材24から研磨工具3に流れる電流は、直接電解液EL中の抵抗R1を経由して研磨工具3に流れる電流i1と、電解液EL中からウェーハWの表面に形成された銅からなる金属膜MTを経由して再度電解液EL中を通して研磨工具3に流れる電流中に流れる電流i2に分岐する。金属膜MTの表面に電流i2が流れるとき、金属膜MTを構成する銅は、電解液ELの電解作用によってイオン化し、電解液EL中に溶出する。

【0047】ここで、電解液EL中の抵抗R1は、陽極としてのスクラップ部材24と陰極としての研磨工具3との距離dに比例して極端に大きくなる。このため、極間距離dを、ギャップδbおよびギャップδwよりも十分に大きくしておくことで、直接電解液EL中の抵抗R1を経由して研磨工具3に流れる電流i1は非常に小さくなり、電流i2が大きくなっている。電解電流のほとんどは金属膜MTの表面を経ることになる。このため、金属膜MTを構成する銅の電解溶出を効率的に行うことができる。また、電流i2の大きさは、ギャップδbおよびギャップδwの大きさによって変化するため、上述したように、コントローラ55によって研磨工具3のZ軸方向の位置制御を行ってギャップδbおよびギャップδwの大きさを調整することにより、電流i2を一定にすることができる。ギャップδwの大きさの調整は、電流信号62sから得られた電解電流、すなわち、電流i2が一定となるように、電流信号62sをフィードバック信号としてZ軸サーボモータ18の制御を行うことである。また、研磨装置1のZ軸方向の位置決め精度は分解能0.1μmと十分に高く、加えて、主軸12

aをウェーハWの正面に対して微小角度で傾斜させていることで実行的な接触面積Sは常に一定に維持されることから、電解電流の値を一定に制御すれば、電流密度は常に一定とでき、金属膜の電解溶出量も常に一定にすることができる。

【0048】以上のように、上記構成の研磨装置1は、上述したウェーハWに形成された金属膜MTを構成する金属を電解液ELによる電解作用によって溶出除去する電解研磨機能を備えている。さらに、上記構成の研磨装置1は、この電解研磨機能に加えて、研磨工具3およびスラリーSLによる通常のCMP装置の化学機械研磨機能も備えており、ウェーハWをこれら電解研磨機能および化学機械研磨の複合作用によって研磨すること(以下、電解複合研磨という)もできる。また、上記構成の研磨装置1は、スラリーSLを用いずに研磨工具3の研磨面3aの機械的な研磨と電解研磨機能との複合作用によって研磨加工を行うこともできる。上記構成の研磨装置1は、電解研磨および化学機械研磨の複合作用によって金属膜を研磨できるため、化学機械研磨のみ、あるいは、機械研磨のみを用いた研磨装置に比べてはるかに高能率に金属膜の除去を行うことができる。金属膜に対する高い研磨レートが得られるため、研磨工具3のウェーハWに対する加工圧力Fを化学機械研磨のみ、あるいは機械研磨のみを用いた研磨装置に比べて低く抑えることが可能となり、ディッシング、エロージョンの発生を抑制することができる。

【0049】以下、本実施形態に係る研磨装置1の電解複合研磨機能を用いた研磨方法について、多層配線構造の半導体装置のデュアルグマシン法による配線形成プロセスに適用した場合を例に説明する。

【0050】図9は、本発明の半導体装置の製造方法の一実施形態に係る製造プロセスを示す工程図であり、図9に示す工程図に基づいて本実施形態に係る製造プロセスを説明する。まず、図10に示すように、たとえば、図示しない不純物拡散領域が適宜形成されている、たとえば、シリコン等の半導体からなるウェーハW上に、たとえば、シリコン酸化膜(SiO₂)からなる層間絶縁膜102を、たとえば、反応源としてTEOS(tetraethylorthosilicate)を用いて減圧CVD(Chemical Vapour Deposition)法により形成する。次いで、図11に示すように、ウェーハの不純物拡散領域に通じるコンタクトホール103およびウェーハWの不純物拡散領域と電気的に接続される所定パターンの配線が形成される。配線用溝104を、たとえば、公知のフォトリソグラフィ技術およびエッチャリング技術を用いて形成する。なお、配線用溝104の深さは、たとえば、800nm程度である。

【0051】次いで、図12に示すように、バリヤ膜105を層間絶縁膜102の表面およびコンタクトホール103、配線用溝104内に形成する。このバリヤ膜3

05は、たとえば、Ta、Ti、TaN、TiN等の材料をスパッタリング装置、真空蒸着装置等を用いたPVD(Physical Vapor Deposition)法により、たとえば、15nm程度の膜厚で形成する。バリヤ膜305は、配線を構成する材料が層間絶縁膜102中に拡散するのを防止するため、および、層間絶縁膜102との密着性を上げるために設けられる。特に、配線材料が銅で層間絶縁膜102がシリコン酸化膜のような場合には、銅はシリコン酸化膜への拡散係数が大きく、酸化されやすいため、これを防止する。以上までのプロセスが図9に示すプロセスPR1である。

【0052】次いで、図13に示すように、バリヤ膜105上に、配線形成材料と同じ材料、たとえば、銅からなるシード膜106を公知のスパッタ法により、たとえば、150nm程度の膜厚で形成する(プロセスPR2)。シード膜106は、銅を配線用溝およびコンタクトホール内に埋め込んだ際に、銅グレインの成長を促すために形成する。次いで、図14に示すように、コンタクトホール103および配線用溝104を埋め込むように、バリヤ膜105上に銅からなる金属膜107を、たとえば、2000nm程度の膜厚で形成する。金属膜107は、好ましくは、電解メッキ法または無電解メッキ法によって形成するが、CVD法、スパッタ法等によって形成してもよい。なお、シード膜106は金属膜107と一緒に一体化する(プロセスPR3)。

【0053】ここで、図15は金属膜107をバリヤ膜105上に形成した製造プロセス途中の半導体装置の断面の拡大図である。図15に示すように、金属膜107の表面には、コンタクトホール103および配線用溝104への埋め込みのために、たとえば、600nm程度の高さの凹凸が発生している。以上のプロセスは、従来と同様のプロセスで行われるが、本発明の研磨方法では、層間絶縁膜102上に存在する余分な金属膜107およびバリヤ膜105の除去を化学機械研磨ではなく、上記の研磨装置1の電解複合研磨によって行う。また、本発明の研磨方法では、上記の電解複合研磨によるプロセスに先立って、図16に示すように、金属膜107の表面に不動態膜108を形成する(プロセスPR4)。この不動態膜108は、金属膜107を構成する金属(銅)の電解反応を妨げる作用を発揮する材料からなる膜である。

【0054】不動態膜108の形成方法は、たとえば、金属膜107の表面に酸化剤を塗布して酸化膜を形成する。金属膜107を構成する金属が銅の場合には、酸化銅(CuO)が不動態膜108となる。また、他の方法として、金属膜107の表面に、たとえば、はっ水膜、油膜、酸化防止膜、界面活性剤からなる膜、キレート剤からなる膜、および、シランカップリング剤からなる膜のいずれかを形成して不動態膜108とすることも可能である。不動態膜108の種類は特に限定されないが、

電気抵抗が金属膜107に対して高く、機械的強度が比較的低く脆い性質のものを使用する。

【0055】次に、本発明の研磨方法では、金属膜107の凸部に形成された不動態膜108のみを選択的に除去する(プロセスPR5)。不動態膜108の選択的な除去は、上記の研磨装置1によって行う。なお、使用するスラリーSLには、銅に対する研磨レートの高いスラリーを用いる。たとえば、過酸化水素、硝酸鉄、ヨウ素酸カリウム等をベースとした水溶液にアルミナ、シリカ、マンガン系の研磨砥粒を含むものを使用する。まず、ウェーハWを研磨装置1のウェーハテーブル42にチャッキングし、電解液ELおよびスラリーSLをウェーハW上に供給しながら回転する研磨工具3およびスラブ部材24をZ軸方向に下降させてウェーハWに接触または接近させ、ウェーハWをX軸方向に所定の速度パターンで移動させて研磨加工を行う。また、研磨工具3にマイナス極、電極板23をプラス極として、研磨工具3と電極板23との間に直流パルス電圧を印加する。なお、スラリーSLのベースとなる水溶液に電解液SLの機能を持たせることにより、スラリーSLのみをウェーハW上に供給してもよい。

【0056】ここで、図17は上記の状態にあるスラブ部材24付近における研磨プロセスを示す概念図であり、図18は研磨工具3付近における研磨プロセスを示す概念図である。図17に示すように、スラブ部材24付近では、回転する電極板23の溝部23bからスラリーSLおよび電解液ELが供給されて、スラリーSLおよび電解液ELはスラブ部材24を通過してスラブ部材24の全面からウェーハW上に供給される。金属膜107上に形成された不動態膜108は、電解液ELによる電解作用を受けないため電解液EL中への金属膜107を構成する銅の溶出は抑制された状態にある。このため、金属膜107には電流がほとんど流れず、上記の電流計62のモニタした電流値は、低く安定したままである。図25は、本実施形態の電解複合研磨プロセスにおいて電流計62でモニターした電流値の一例を示すグラフである。図25に示す電流値の開始位置付近が上記の状態である。

【0057】スラブ部材24の回転にしたがって、機械的除去作用あるいはスラリーSLに含まれる、たとえば、酸化アルミニウムからなる研磨砥粒PTの機械的除去作用によって不動態膜108の高い部分、すなわち、金属膜107の凸部上の不動態膜108から機械的に除去されていく。一方、図18に示すように、研磨工具3付近では、研磨工具3の機械的除去作用、あるいは、研磨砥粒PTの機械的除去作用によって金属膜108に存在する不動態膜108が高い部分から除去される。

【0058】このようにして、たとえば、図19に示すように、金属膜107の凸部上に形成された不動態膜108が選択的に除去されると、不動態膜108が選択的

に除去された部分から金属膜107が表面に露出する。【0059】金属膜107が表面に露出すると、凸部である金属膜107の露出部分が選択的に溶出する(プロセスPR5)。このときの電解液ELの作用は、図18に示すように、不動態膜108が除去された部分である金属膜107の凸部は、金属膜107を構成する銅が電解作用によって銅イオンCu⁺として電解液EL中に溶出する。これによって、金属膜107中にはマイナス電子e⁻が流れ、このマイナス電子e⁻は、図17に示したように、金属膜107の表面から電解液ELを通して電極板23に流れ、上記した電流i₂となる。

【0060】上述したように、金属膜107を構成する銅は、不動態膜108に比べて電気抵抗が低く電流密度が増すため、集中的な電解作用を受け選択的に溶出がおこり、材料除去が加速される。また、電解液ELを介して通電するため、陽極としての金属膜107と陰極としての研磨工具3の電位差が一定の場合、極間距離が短い、すなわち、電気抵抗値が低いほうが極間に流れる電流値は大きくなる。このため、陰極としての研磨工具3に対して、陰極としての金属膜107の凹凸による電極間距離の差(金属膜107の凸部のなかでも高い部分のほうが極間距離が短く電気抵抗が低い)があれば、電流密度の違いから高い順に溶出速度が大きくなる効率的な平坦化が進行する。このとき、図25において、P1で示すように、上記の電流計62のモニタした電流値は上昇しはじめる。このような作用によって、金属膜107の凸部は、機械的平坦化に比べて、はるかに高能率に平坦化が行われる。

【0061】上記の作用によって、金属膜107の凸部がほぼ完全に平坦化されるまで選択的な電解複合研磨が完了した金属膜107の表面は、たとえば、図20に示すように、金属膜107の凹部であった部分に残存する不動態膜108と金属膜107の凸部が除去された銅の新生面の複合面になる。

【0062】続いて、図21に示すように、この金属膜107の表面に研磨工具3およびスラリーSL中の研磨砥粒PTにより行われる機械的除去と電解液ELによる電解作用が複合した電解複合研磨が進行する(プロセスPR7)。このとき、残存する不動態膜108の機械的強度は上述したように銅の新生面に比べて低いため、不動態膜108が電解複合研磨されるとき、主に機械的作用により除去され、その下にある銅表面が露出し、その面積に比例して電解作用が増大する。不動態膜108が完全除去された時点で金属膜107を構成する銅の表面積は最大となる。これと同時に、電流計62でモニタした電流は、図25においてP1の位置から上昇した電流値は、不動態膜108の除去に伴って上昇した後、銅の表面積が最大となるP2で示す時点で最大値となる。ここまでプロセスによって、金属膜107の表面の初期凹凸の平坦化は完了する。

【0063】このように、本実施形態の電解複合研磨は、電気化学的に研磨レートをアシストされた研磨であるため、通常の化学機械研磨に比べて低い加工圧力で研磨を行うことができる。このことは、単純な機械的研磨として比較してもスクラッチの低減、段差緩和性能、ディッシングやエロージョンの低減などの面で非常に有利である。さらに、低い加工圧力で研磨を行うことができるため、機械強度が低く通常の化学機械研磨では破壊されてしまいやすい、有機系の低誘電率膜や多孔質低誘電率絶縁膜を層間絶縁膜102に用いていた場合に非常に有利である。

【0064】上記の金属膜107の電解複合研磨が進行して、余分な金属膜107が除去されると、図22に示すように、バリア膜105が露出する(プロセスP8)。このとき、電流計62のモニターする電流は、図25のP2で示す金属膜107上の不動態膜108がすべて除去された時点より最大値をとり、図25のP3で示すバリア膜105が露出する時点まで略一定の値をとる。バリア膜105が露出すると、たとえば、Ta、Ti、TaN、TiN等の材料を使用した場合には、その電気抵抗が銅に比べ大きいため、たとえば、図25のバリア膜105の露出が開始するP3で示す時点から電流計62でモニターした電流値が低下しはじめる。この状態では、金属膜107の不均一分の銅膜が残留する状態であり、この状態で研磨加工を一旦停止する。この研磨加工の停止は、図25のP4で示すように電流値が所定の値まで下がったことをコントローラ55が判断し、研磨装置1の研磨動作を停止させる。

【0065】次いで、バリア膜105を除去する(プロセスPR9)。このバリア膜105を除去するプロセスでは、上記の銅から構成される金属膜107に対して研磨レートの高いスラリーSLではなく、Ta、TaN、Ti、TiN等の材料から形成されたバリア膜105に対して研磨レートが高く、金属膜107に対して研磨レートの低いスラリーSLを使用する。すなわち、バリア膜105と金属膜107の研磨レートの選択比ができるだけ大きなスラリーSLを使用する。

【0066】さらに、オーバーポリッシュによるディッシング、エロージョンの発生を抑制する観点等から、電解電源61の出力電圧を上記のプロセスよりも小さくしてバリア膜105の研磨除去を行う。また、研磨工具3の加工圧力も上記のプロセスよりも小さくするのが好ましい。また、電解電源61の出力電圧を小さくすること、および、バリア膜105を除去すると層間絶縁膜102が表面に露出することから、電解電流の値は小さくなるので、上記の電流計62による電解電流のモニタに代えて、上記の抵抗計63によってスクラブ部材24と研磨工具3との間に電気抵抗をモニターする。

【0067】バリア膜105を除去すると、図23に示すように、層間絶縁膜102が表面に露出する(プロセス

SP10)。層間絶縁膜102が露出すると、図23に示すように、この露出部分には、陽極として表面に通電するための金属膜107やバリア膜105がないため、スクラップ部材24による通電が遮断され、層間絶縁膜102の露出部分での電解作用が停止する。このとき、抵抗計63によってモニターした電気抵抗値は増加はじめる。

【0068】ここで、金属膜107の残存する部分とバリア膜105の露出部分との間で、上記した金属膜107の凸部の段差緩和の場合と同様に、すなわち、不動態膜108の代りにバリア膜105を電気抵抗の高い部分として、金属膜107の残存部分への電流密度の集中がおこり選択的に金属膜107の残存部分は溶出除去される。電解作用の停止した部分には、研磨工具3とスラリーSLによる機械的な材料除去作用のみが主体的に働く。

【0069】ところで、通常の化学機械研磨では、バリア膜105および金属膜107の層間絶縁膜102に対する研磨レート選択比ができるだけ大きくし、そのレート差をマージンとして層間絶縁膜102の上面の寸法精度を確保しようとしている。このため、金属膜107のディッシングは避けられない構成となっている。また、選択比を低く設定すればディッシングはある程度少なくすることができるが、寸法精度は、ウェーハ面内除去量分布の均一性に依存するため、バリア膜105および金属膜107の除去が十分ではない場合も発生する。このため、バリア膜105および金属膜107が層間絶縁膜102の上面に残存した状態であるアンダーポリッシュを防ぐためには、除去量の面内不均一分のオーバーポリッシュが必要となり、このオーバーポリッシュによるエロージョンの悪化は本質的に避けられない。一方、本実施形態では、ウェーハWの面内均一性をある程度確保しておけば、層間絶縁膜102上に残るバリア膜105、あるいは、金属膜107の残存部分には電解作用が働くことで高能率除去され、層間絶縁膜102の露出部分から溶出が停止する。このため、層間絶縁膜102の寸法精度は自動的に確保され、ディッシング、エロージョンの発生が抑制される。

【0070】上記のようにして、たとえば、Ta、Ta_N、Ti、TiN等の材料から形成されたバリア膜105を完全に除去することができるとともに、オーバーポリッシュによるディッシング、エロージョンの発生を抑制することができる。また、上述したバリア膜105の除去プロセスでは、絶対電流値は低く、機械的負荷も軽く設定することで除去速度は遅くなるが、残存する膜厚が不均一な部分の残留分の銅膜からなる金属膜107が少なければ、バリア膜105は金属膜107に比べて薄いためバリア膜105の除去量自体は小さく、このプロセスにおいてバラツキ・不均一があったとしてもディッシング、エロージョンの絶対値は無視できる程度に少ない。

ぐで、処理時間も短くすることができる。さらに、本実施形態に係る研磨方法は、機械的研磨に加えて電気化学的作用が付加された複合加工であるため、平坦化した表面はダメージが少なく機械的にも平滑な面を得ることができる。

【0071】次いで、抵抗計63でモニターした電気抵抗値に基づいて、電気抵抗値が最大値すなわち配線形成が完了した時点でバリア膜105を除去するプロセスを終了する(プロセスPR11)。コントローラ55は電気抵抗値の値を判断して、研磨装置1の加工動作を停止させる。なお、研磨加工を終了する前に、電解作用を附加したままの状態で、研磨工具3をウェーハWの表面に接触させず、例えば、100μm程度上を通過させることで、機械的研磨は行わず、電解作用のみによるダメージフリーの表面を形成することができる。これにより、図23に示すように、層間絶縁膜102中には配線109およびコンタクト110が最終的に形成される。

【0072】次いで、配線109およびコンタクト110が形成された半導体装置に対してフラッシングを行う(プロセスPR12)。このフラッシングプロセスは、配線109およびコンタクト110が形成された後、直ぐに洗浄薬液、酸化防止剤をウェーハWの表面に供給しながら、ウェーハWには通電せず、図24に示すように、研磨工具3にプラスのパルス電圧を印加し、純水洗浄、薬液洗浄を行い、ウェーハWの表面に存在するスラリーSLやパーティクルを除去する。本実施形態では、フラッシングを行う以前にも、スラリーSLに含まれる、たとえば、アルミナからなる研磨砥粒PTは分散性をよくするために正に帯電させているため、銅からなる金属膜107表面に機械的に衝突して除去加工に寄与したのち摩滅せずに残留した場合にも、陽極としての金属膜107を構成する銅の表面に埋没することはない、図23に示したように、陰極としての研磨工具3の表面に再付着して次の加工に寄与する。さらに、正に帯電したパーティクルも陰極としての研磨工具3の表面に引き寄せられるため、銅の表面に埋没することはない。一方、ウェーハWの表面に残存して負に帯電しているパーティクルも上記のフラッシングによって、ウェーハWの表面から除去することができる。また、研磨砥粒PTが負に帯電したスラリーSLを使用した場合にも同様に除去できる。配線形成材料が銅である場合、酸化されやすく、銅表面を変質させずに、金属イオンやパーティクルを除去する必要があるが、本実施形態では、予め研磨砥粒PTを正に帯電させておき、かつ、フラッシングによってこの問題が解消される。なお、研磨砥粒として、酸化アルミニウム(アルミナ)を例として挙げたが、酸化セリウム、シリカ、酸化ゲルマニウムなどを使用した場合にも同様である。

【0073】以上のように、本実施形態に係る半導体装置の製造方法によれば、絶縁膜102内に形成した配線

用溝配線およびコンタクトホールを埋め込む金属膜107に不動態膜108を形成し、金属膜107の凸部に形成された不動態膜108を選択的に除去し、残った不動態膜108をマスクとして表面に露出した金属膜107を電解研磨によって選択的に除去し、かつ電流密度に集中によって集中的に除去することで、通常のCMPに比べてはるかに高能率に初期凹凸を平坦化することができる。また、初期凹凸が平坦化された金属膜107は、電解研磨と化学機械研磨の複合した電解複合研磨によって除去されるため、通常のCMPに比べてはるかに高能率に余分な金属膜107を除去できる。このため、研磨工具3の加工圧力を低く設定しても十分な研磨レートが得られ、金属膜107へのダメージを軽減できるとともに、ディッシングやエロージョンの発生を抑制することができる。

【0074】また、本実施形態に係る半導体装置の製造方法によれば、余分な金属膜107を除去してバリヤ膜105が露出した時点で、研磨を停止し、スラリーSLをバリヤ膜105に対して研磨レートの高いものに変更し、電解電源61の出力電圧等の研磨条件を変更して余分なバリヤ膜105を除去を行うため、余分なバリヤ膜105を確実に除去でき、オーバボリッシュが必要な場合にも、ディッシングやエロージョンの発生量を小さく抑えることができる。

【0075】また、本実施形態に係る半導体装置の製造方法によれば、金属膜の研磨を電解複合研磨によって高能率に行うため、研磨工具3の加工圧力を低圧力にすることができるため、たとえば、低消費電力化および高速化等の観点から誘電率を低減するために層間絶縁膜102として機械的強度が比較的低い有機系低誘電率膜や多孔質低誘電率絶縁膜を使用した場合にも、これらの絶縁膜へのダメージを低減することができる。

【0076】上述した実施形態では、金属膜の研磨加工量の絶対値は、電解電流の積算量と研磨工具3のウェーハWを通過する時間で制御できる。上述した実施形態では、銅による配線形成プロセスの場合を説明したが、本発明はこれに限定されることなく、タンクステン、アルミニウム、銀等の種々の金属配線形成プロセスに適用可能である。

【0077】また、上述した実施形態では、スラリーSLを用いた化学機械研磨と電解液ELを用いた電解研磨とを複合した電解複合研磨の場合について説明したが、本発明はこれに限定されない。すなわち、本発明は、スラリーSLを用いずに、電解液ELの電解研磨と研磨工具3の研磨面3aによる機械研磨によって電解複合研磨を行うことも可能である。

【0078】また、上述した実施形態では、研磨工具3と電極板23との間を流れる電流値をモニターし、この値に基づいてバリヤ膜105が露出するまでの研磨プロセスを管理したが、全ての研磨プロセスをモニターした。

電流値で管理することも可能である。同様に、上述した実施形態では、研磨工具3と電極板23との間の電気抵抗値をモニターし、この値に基づいて、バリヤ膜105の除去プロセスのみの管理を行う構成としたが、全ての研磨プロセスをモニターした電気抵抗値で管理することも可能である。

【0079】変形例1

図26は、本発明に係る研磨装置の一変形例を示す概略図である。上述した実施形態に係る研磨装置1では、ウェーハW表面への通電を、導電性の研磨工具と、スクラップ部材24を備えた通電板23によって行った。図26に示すように、ホイール状の研磨工具401は、研磨装置1の場合と同様に導電性を持たせるとともに、ウェーハWをチャッキングし回転させるウェーハテーブル402にも導電性を持たせる構成としてもよい。研磨工具401への給電は、上述した実施形態と同様の構成で行う。この場合には、ウェーハテーブル402への通電は、ウェーハテーブル402の下部にロータリージョイント403を設け、ロータリージョイント403によって回転するウェーハテーブル402への通電を常に維持する構成とすることで、電解電流の供給を行うことができる。

【0080】変形例2

図27は、本発明に係る研磨装置の他の変形例を示す概略図である。ウェーハWをチャッキングし、回転させるウェーハテーブル502は、ウェーハWをウェーハWの周囲に設けたリテナーリング504によって保持している。研磨工具501には、導電性を持たせるとともに、リテナーリング504にも導電性を持たせ、研磨工具501には上述した実施形態と同様の構成で給電する。また、リテナーリング504は、ウェーハWに形成された上記のバリア層部分まで覆い通電する。さらに、リテナーリング504には、ウェーハテーブル502の下部に設けられたロータリージョイント503を通じて給電する。なお、研磨工具501がウェーハWに接触しても、エッジの部分でリテナーリング504の厚さ以上の隙間が維持できるように研磨工具3の傾斜量を大きくしておくことで、研磨工具501とリテナーリング504との干渉を防ぐことができる。

【0081】変形例3

図28は、本発明に係る研磨装置の他の実施形態を示す概略構成図である。図28に示す研磨装置は、従来型のCMP装置に本発明の電解研磨機能を附加したものであって、定盤201上に研磨パッド（研磨布）202が貼着された研磨工具の研磨面にウェーハチャック207によってチャッキングされたウェーハWの全面を回転させながら接触させてウェーハWの表面を平坦化する研磨装置である。研磨パッド202には、陽極電極204と陰極電極203とが放射状に交互に配置されている。また、陽極電極204と陰極電極203とは絶縁体206

によって電気的に絶縁されており、陽極電極204と陰極電極203は、定盤201側から通電される。これら陽極電極204と陰極電極203と絶縁体206によって研磨パッド202は構成されている。また、ウェーハチャック207は、絶縁材料から形成されている。さらに、この研磨装置には、研磨パッド202の表面に電解液E-LおよびスラリーSLを供給する供給部208が設けられており、電解研磨および化学機械研磨を複合させた電解複合研磨が可能になっている。

【0082】ここで、図29は、上記構成の研磨装置による電解複合研磨動作を説明するための図である。なお、ウェーハW表面には、たとえば、銅膜210が形成されているものとする。図29に示すように、電解複合研磨中には、ウェーハW表面に形成された銅膜210と研磨パッド202の研磨面との間には、電解液E-LおよびスラリーSLが介在した状態で、陽極電極204と陰極電極203との間に直流電圧が印加され、電流iが陽極電極204から電解液E-Lを通って銅膜210内を伝って再び電解液E-Lを通って陰極電極203に流れる。このとき、図29に示す円G内の付近では、電解作用によって銅膜210が溶出するとともに、銅膜210は研磨パッド202とスラリーSLによる機械的除去作用によってさらに除去される。

【0083】このような構成とすることにより、上述した実施形態に係る研磨装置1と同様の効果が奏される。なお、研磨パッドに設ける陽極電極、陰極電極の配置は図28の構成に限定されるわけではなく、たとえば、図30に示すように、線状の複数の陽極電極222を縦横に等間隔に配列し、陽極電極222によって囲まれる各矩形領域に陰極電極223を配置し、陽極電極222と陰極電極223とを絶縁体224で電気的に絶縁した研磨パッド221としてもよい。さらに、たとえば、図31に示すように、半径がそれぞれ異なる環状の陽極電極242を同心上に配置し、各陽極電極242間に形成される環状領域に陰極電極243をそれぞれ配置し、陽極電極242と陰極電極243とを絶縁体244で電気的に絶縁した研磨パッド241としてもよい。

【0084】

【発明の効果】本発明によれば、機械研磨と電解研磨との複合作用によって金属膜を研磨するので、機械研磨による金属膜の平坦化の場合に比べて、非常に高能率に金属膜の凸部の選択的除去および平坦化が可能となる。また、本発明によれば、研磨工具を陰極として通電するため、予め正に帯電したパーティクルや研磨剤中の研磨砥粒が研磨工具に引き寄せられ、ウェーハ表面へ残留するのを防止することができ、歩留りの向上を図ることができる。また、本発明によれば、高能率に金属膜の除去が可能となるので、比較的低い研磨圧力でも十分な研磨レートが得られ、研磨した金属膜にスクラッチ、ディッシング、エロージョン等が発生するのを抑制することができる。

きる。さらに、本発明によれば、比較的低い研磨圧力でも十分な研磨レートが得られため、半導体装置の低消費電力化および高速化等の観点から誘電率を低減するために層間絶縁膜として機械的強度が比較的低い有機系低誘電率膜や多孔質低誘電率絶縁膜を使用した場合にも、容易に適用可能である。また、本発明によれば、層間絶縁膜上に残るパリヤ膜、あるいは、金属の部分は電解作用が働くことで効率的に除去され、絶縁膜の露出部分から溶出が停止するため、研磨の停止精度を自動的に確保することができ、ディッシング、エロージョンを抑制することができる。また、本発明によれば、電解電流をモニタリングすることで、研磨プロセスの管理を行うことができ、研磨プロセスの進行状態を正確に把握することができる。また、本発明によれば、研磨工具と電極部材との間の電気抵抗値をモニタリングすることで、電流が流れにくい、または電流が流れない膜と金属膜とを同時に研磨するような場合でも、研磨プロセスを正確に管理することができる。

【図面の簡単な説明】

【図1】本発明の研磨装置の一実施形態の構成を示す図である。

【図2】図1の研磨装置のヘッド部の詳細を示す拡大図である。

【図3】(a)は電極板23の構造の一例を示す下面図であり、(b)は電極板23と、通電軸20、スクラップ部材24および絶縁部材4との位置関係を示す断面図である。

【図4】研磨工具とウェーハとの関係を示す図である。

【図5】研磨工具に対してウェーハをX軸方向に移動させた様子を示す図である。

【図6】ヘッド加工部でウェーハを研磨加工する状態を示す概略図である。

【図7】研磨工具と電極板との関係を示す図である。

【図8】本発明の研磨装置の電解研磨機能を説明するための図である。

【図9】本発明の半導体装置の製造方法の一実施形態に係る製造プロセスを示す工程図である。

【図10】本発明の半導体装置の製造方法の製造プロセスを示す断面図である。

【図11】図10に続く製造プロセスを示す断面図である。

【図12】図11に続く製造プロセスを示す断面図である。

【図13】図12に続く製造プロセスを示す断面図である。

【図14】図13に続く製造プロセスを示す断面図である。

【図15】図14に示す半導体装置の断面構造の拡大図である。

【図16】図14に示す半導体装置の断面構造の拡大図である。

る。

【図17】スクラブ部材24付近における研磨プロセスを示す概念図である。

【図18】研磨工具3付近における研磨プロセスを示す概念図である。

【図19】図16に続く製造プロセスを示す断面図である。

【図20】金属膜の凸部が選択的に除去され平坦化された状態を示す断面図である。

【図21】図19に続く製造プロセスを示す断面図である。

【図22】図21に続く製造プロセスを示す断面図である。

【図23】図22に続く製造プロセスを示す断面図である。

【図24】研磨加工が終了した半導体装置に対してフラッシングをした状態を示す断面図である。

【図25】電解複合研磨プロセスにおいてモニターした電流値の一例を示すグラフである。

【図26】本発明の研磨装置の変形例を示す図である。

【図27】本発明の研磨装置のさらに他の変形例を示す図である。

【図28】本発明に係る研磨装置の他の実施形態を示す概略構成図である。

【図29】図28に示した研磨装置による電解複合研磨動作を説明するための図である。

【図30】研磨パッドの電極構成の他の例を示す図であ

る。

【図31】研磨パッドの電極構成のさらに他の例を示す図である。

【図32】デュアルダマシン法による配線形成プロセスを示す断面図である。

【図33】図32に続く配線形成プロセスを示す断面図である。

【図34】図33に続く配線形成プロセスを示す断面図である。

【図35】図34に続く配線形成プロセスを示す断面図である。

【図36】図35に続く配線形成プロセスを示す断面図である。

【図37】図36に続く配線形成プロセスを示す断面図である。

【図38】CMP法による金属膜に研磨加工において発生するディッシングを説明するための断面図である。

【図39】CMP法による金属膜に研磨加工において発生するエロージョンを説明するための断面図である。

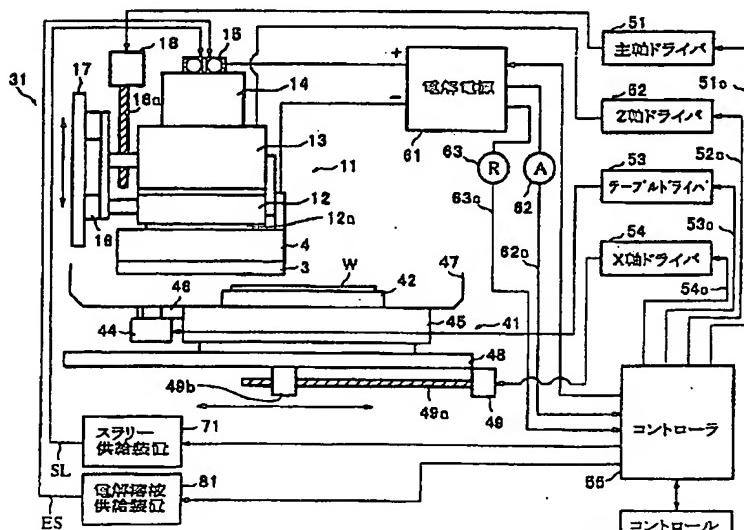
【図40】CMP法による金属膜に研磨加工において発生するリセスを説明するための断面図である。

【図41】CMP法による金属膜に研磨加工において発生する

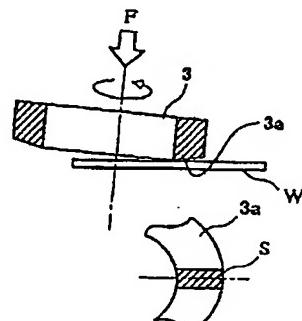
【符号の説明】

- 1…研磨装置、11…加工ヘッド部、61…電解電源、
55…コントローラ 55、71…スラリー供給装置、8
1…電解液供給装置。

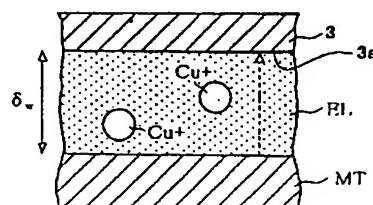
【図1】



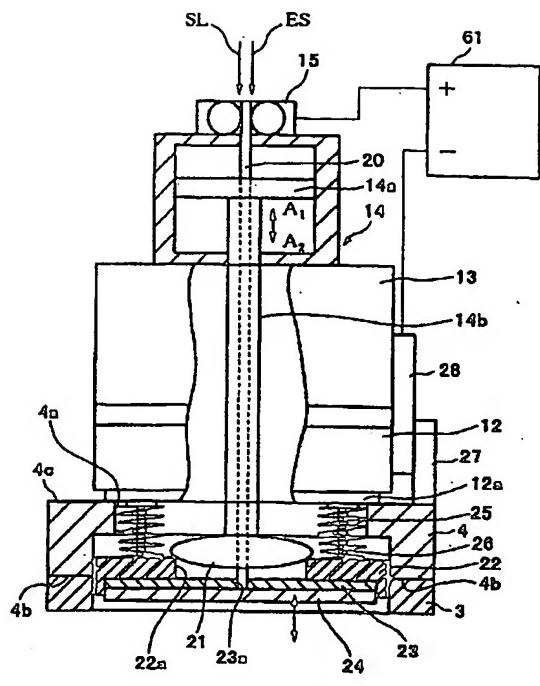
【図4】



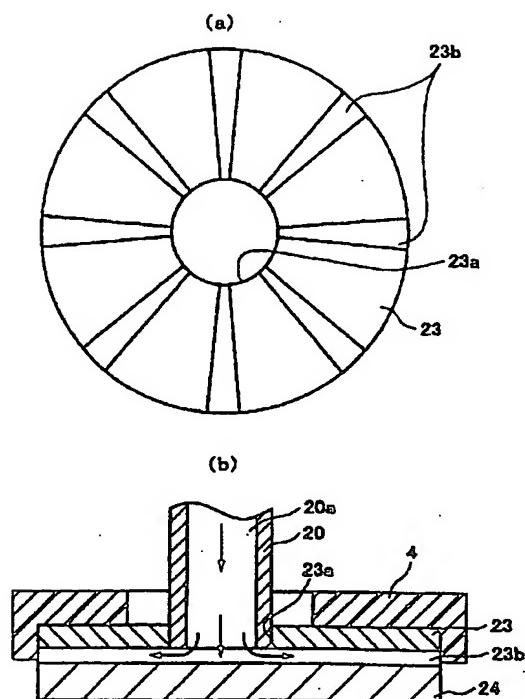
【図8】



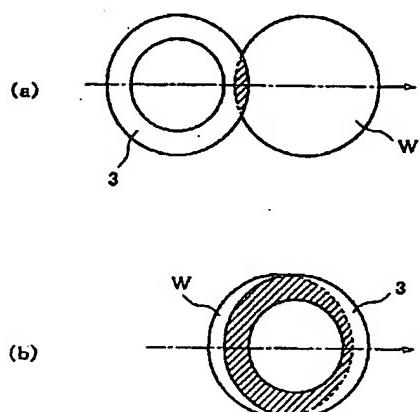
【図2】



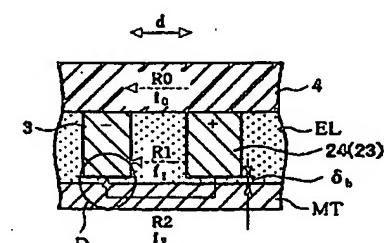
【図3】



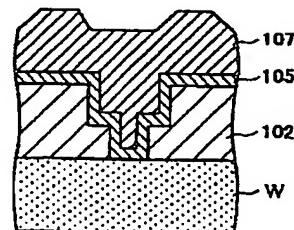
【図5】



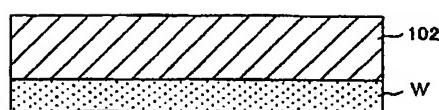
【図7】



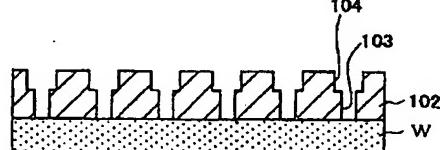
【図15】



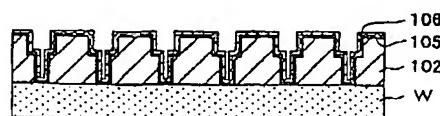
【図10】



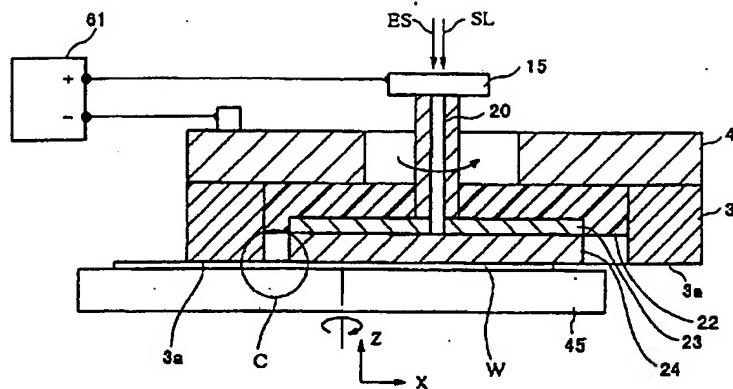
【図11】



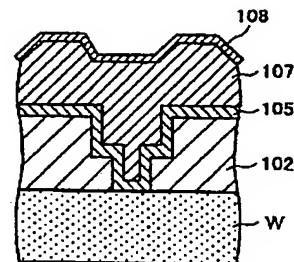
【図13】



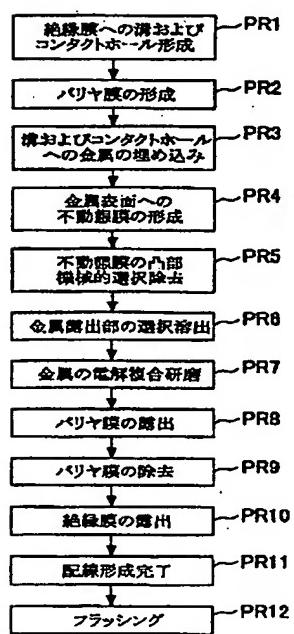
【図6】



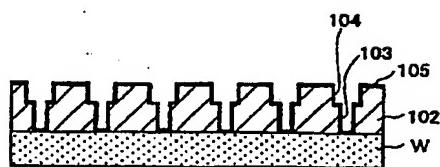
【図16】



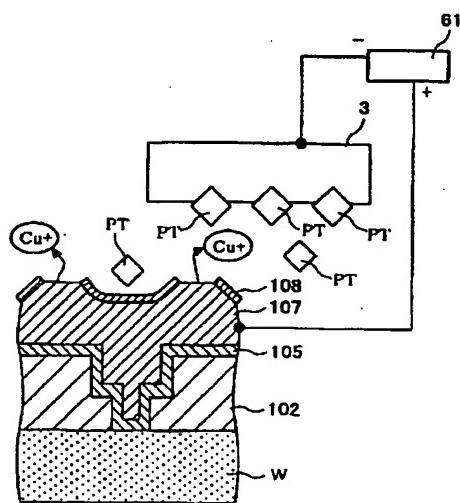
【図9】



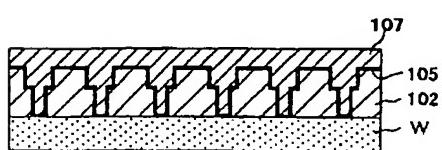
【図12】



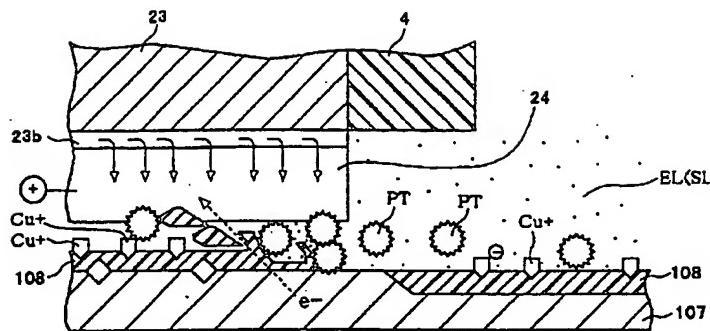
【図19】



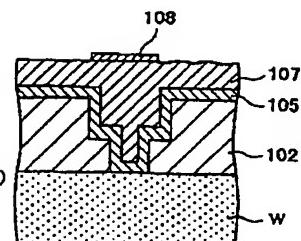
【図14】



【図17】

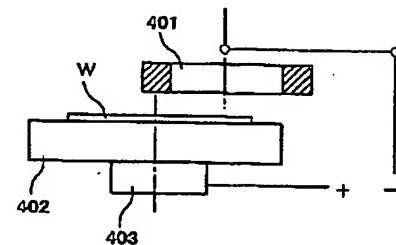
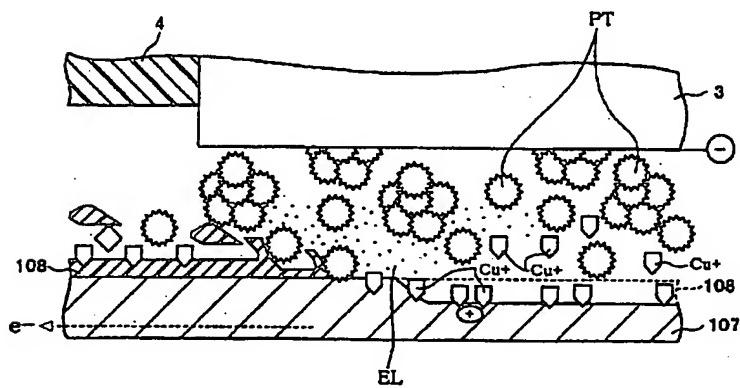


【図20】

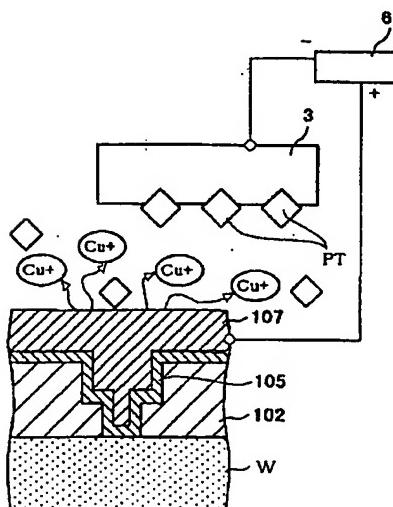


【図26】

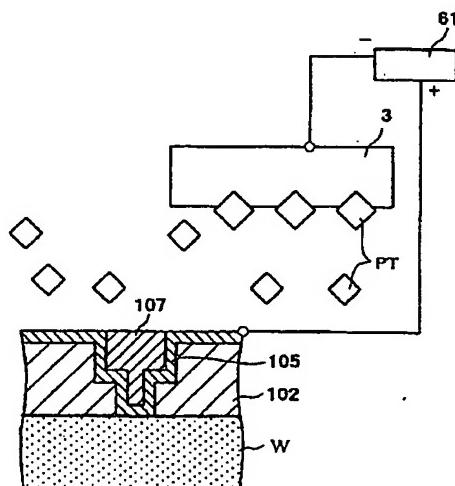
【図18】



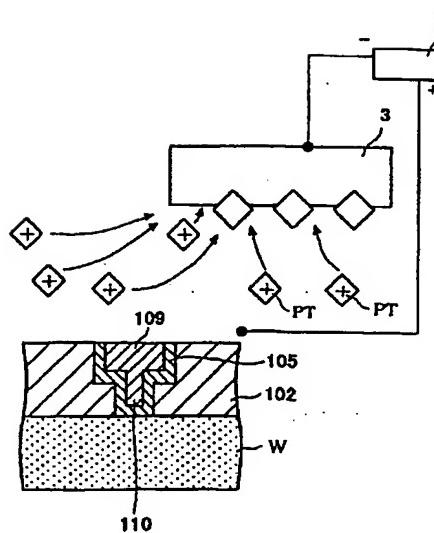
【図21】



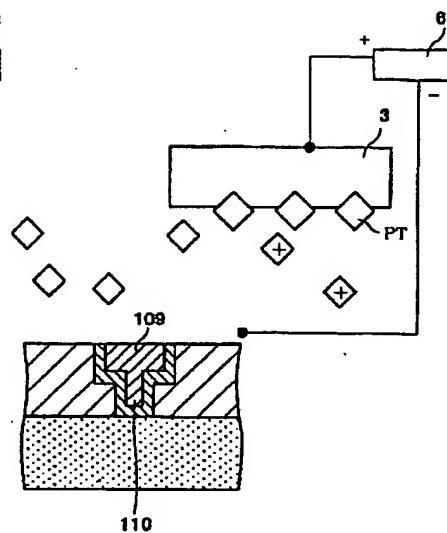
【図22】



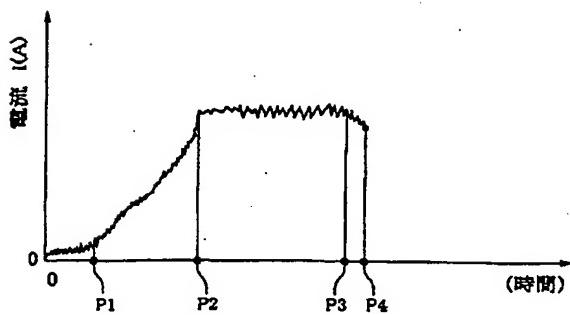
【図23】



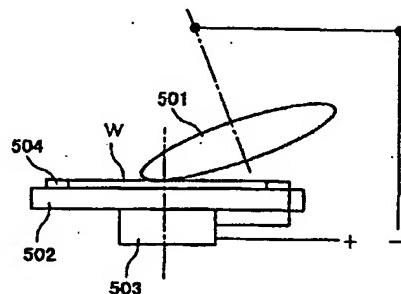
【図24】



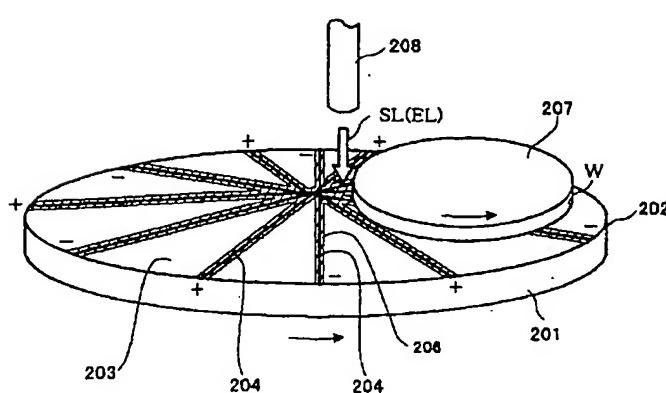
【図25】



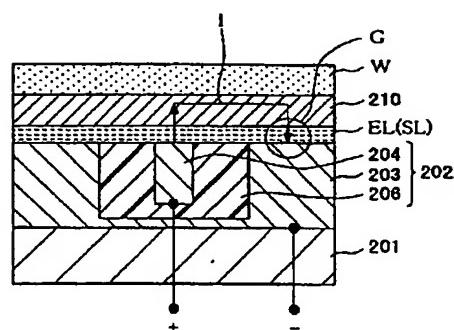
【図27】



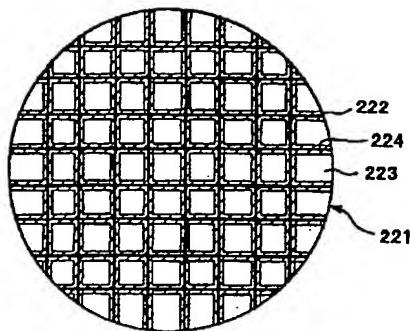
【図28】



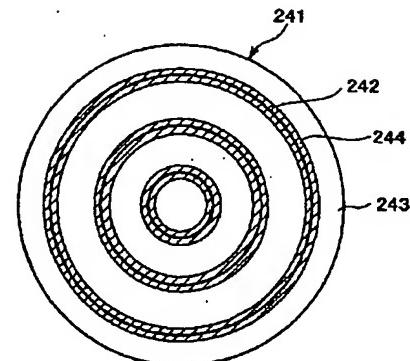
【図29】



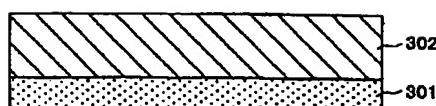
【図30】



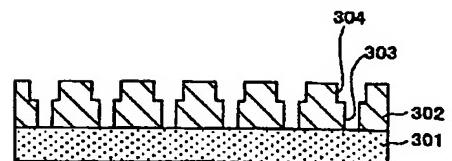
【図31】



【図32】



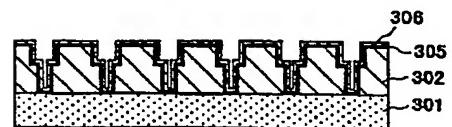
【図33】



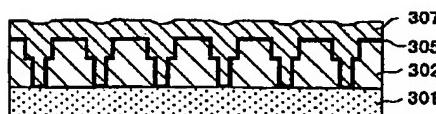
【図34】



【図35】



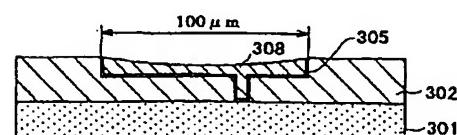
【図36】



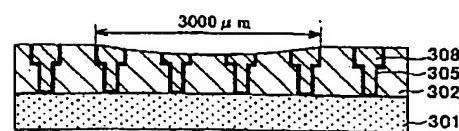
【図37】



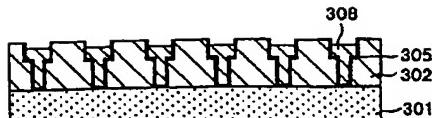
【図38】



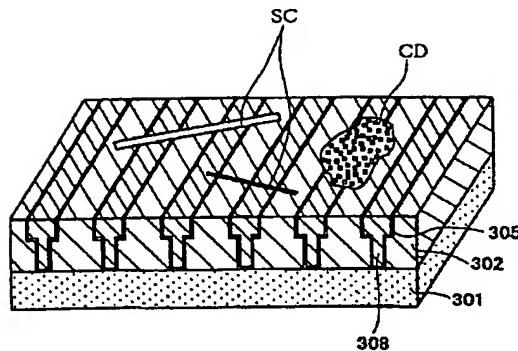
【図39】



【図40】



【図41】



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識別記号

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マーク(参考)

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PP19 PP27 PP28 PP33 QQ09
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SS04 SS13 XX01
5F040 DC01 EJ03 EJ08 FC10
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EE40 FF07 GG10
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SEMICONDUCTOR DEVICE MANUFACTURING METHOD, POLISHING DEVICE, AND
POLISHING METHOD

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[There are no amendments to this patent.]

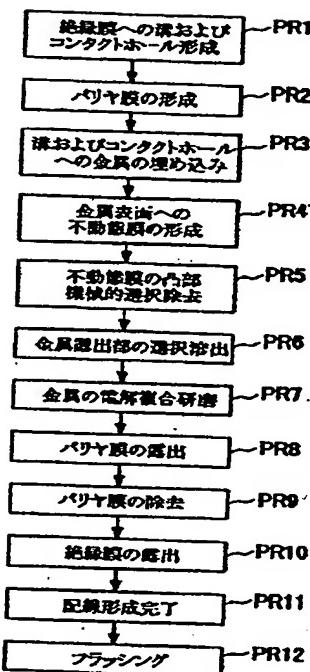
Abstract

Objective

To provide a polishing method, polishing device, and semiconductor device manufacturing method, which can prevent dishing and erosion during a planarization process carried out by polishing a metal film used for forming the wiring of a semiconductor device with a multi-layer wiring structure.

Means to solve

The method has a step for forming a passive film on the surface of a metal film to hinder electrolytic reaction of the metal (PR4), a step in which the passive film on projections existing on the surface of the metal film due to burying of wiring grooves is selectively removed by means of mechanical polishing to expose projections of the metal film on the surface (PR5), a step in which the exposed projections of the metal film are removed by means of electrolytic polishing to planarize the bumps and dips formed on the surface of the metal film due to burying of wiring grooves (PR6), and a step in which the metal film existing on the insulating film (of the planarized metal surface film) is removed by means of composite electrolytic polishing that combines electrolytic polishing and mechanical polishing to form the aforementioned wiring (PR7).



- Key:**
- PR1 Form grooves and contact holes on an insulating film
 - PR2 Form barrier film
 - PR3 Bury metal in the grooves and contact holes
 - PR4 Form passive film on the metal surface
 - PR5 Selectively remove projections of the passive film by means of mechanical polishing
 - PR6 Selectively elute metal projections
 - PR7 Composite electrolytic polishing of the metal
 - PR8 Expose the barrier film
 - PR9 Remove the barrier film
 - PR10 Expose the insulating film
 - PR11 Complete formation of the wiring
 - PR12 Flashing

Claims

1. A semiconductor device manufacturing method having a step in which wiring grooves used for forming wiring are formed on an insulating film formed on a substrate, a step in which a metal film is deposited on the aforementioned insulating film to bury the aforementioned wiring grooves, a step in which a passive film for hindering electrolytic reaction of the metal film is formed on the surface of the metal film deposited on the aforementioned insulating film,

a step in which the passive film on projections existing on the surface of the aforementioned metal film due to burying of the aforementioned wiring grooves is selectively removed by means of mechanical polishing to expose projections of the metal on the surface, and

a step in which the exposed projections of the aforementioned metal film are removed by means of electrolytic polishing to planarize bumps and dips formed on the surface of the aforementioned metal film due to burying of the aforementioned wiring grooves.

2. The semiconductor device manufacturing method described in Claim 1 characterized by having a further step in which excess metal film existing on the insulating film of the planarized metal film is removed by means of composite electrolytic polishing that combines electrolytic polishing and mechanical polishing to form the aforementioned wiring.

3. The semiconductor device manufacturing method described in Claim 2 characterized by the fact that said composite electrolytic polishing combines electrolytic polishing and chemical polishing.

4. The semiconductor device manufacturing method described in Claim 2 characterized by the following facts: after the aforementioned wiring grooves are formed, a barrier film made of an electroconductive material for preventing diffusion of the aforementioned metal film into the aforementioned insulating film is formed to cover the aforementioned insulating film and the aforementioned grooves; after projections of the aforementioned exposed metal film are planarized, excess metal film on the aforementioned insulating film is removed by means of said composite electrolytic polishing until the barrier film is exposed at the surface;

the barrier film existing on the aforementioned insulating film is removed by means of said composite electrolytic polishing until the aforementioned insulating film is exposed at the surface.

5. The semiconductor device manufacturing method described in Claim 4 characterized by the following facts: an electrolyte is placed between the polishing surface of an electroconductive polishing tool and the aforementioned passive film; with the aforementioned metal film and barrier film used as anode and with the aforementioned polishing tool used as cathode, a voltage is applied between the aforementioned metal film, barrier film and the aforementioned polishing tool;

the aforementioned polishing tool is moved with respect to the surface of the passive film to selectively remove the passive film formed on projections of the aforementioned metal film;

the projections of the metal film exposed from the selectively removed passive film are eluted under the electrolytic effect of the aforementioned electrolyte.

6. The semiconductor device manufacturing method described in Claim 5 characterized by the following facts: the electrode part used for applying the voltage to the aforementioned

polishing tool is brought into contact with the aforementioned metal film and barrier film or in vicinity thereof to conduct electricity to the aforementioned metal film and barrier film; the current flowing from the aforementioned electrode part to the aforementioned polishing tool via the aforementioned metal film and barrier film is monitored; and the polishing progress of the aforementioned metal film and barrier film can be controlled based on the magnitude of conventional current.

7. The semiconductor device manufacturing method described in Claim 5 characterized by the following facts: the electrode part used for applying the voltage to the aforementioned polishing tool is brought into contact with the aforementioned metal film and barrier film or in the vicinity thereof to conduct electricity to the aforementioned metal film and barrier film;

the electrical resistance occurring between the aforementioned electrode part and the aforementioned polishing tool is monitored; and the polishing progress of the aforementioned metal film and barrier film can be controlled based on the magnitude of the aforementioned electrical resistance.

8. The semiconductor device manufacturing method described in Claim 5 characterized by the fact that a chemical polishing agent containing abrasive particles is placed between the polishing surface of the aforementioned polishing tool and the aforementioned passive film to selectively remove the aforementioned passive film.

9. The semiconductor device manufacturing method described in Claim 5 characterized by the fact that chemical polishing agents that show different polishing rates with respect to the materials of the aforementioned metal film and barrier film, respectively, are used to remove the aforementioned excess metal film and barrier film.

10. The semiconductor device manufacturing method described in Claim 5 characterized by the fact that in the step for removing the aforementioned excess barrier film, the voltage applied between the aforementioned barrier film and the aforementioned polishing tool is less than the voltage applied between the aforementioned metal film and the aforementioned polishing tool in the step for removing the aforementioned excess metal film.

11. The semiconductor device manufacturing method described in Claim 2 characterized by the fact that the step for forming the aforementioned wiring grooves has a step in which contact holes used for connecting the impurity diffusion layer or wiring formed below the aforementioned insulating film to the wiring formed on the insulating film are formed together with the aforementioned wiring grooves, and

metal is also buried in the aforementioned contact holes as well as in the aforementioned wiring grooves in the step for burying metal in the aforementioned wiring grooves.

12. The semiconductor device manufacturing method described in Claim 11 characterized by the fact that copper is used to form the aforementioned wiring, and that the

copper is buried in the aforementioned wiring grooves and contact holes with an electroplating method.

13. The semiconductor device manufacturing method described in Claim 4 characterized by the fact that the material of the aforementioned barrier film is Ta, Ti, TaN, or TiN.

14. The semiconductor device manufacturing method described in Claim 1 characterized by the fact that the aforementioned passive film is an oxide film formed by oxidizing the surface of the aforementioned metal film.

15. The semiconductor device manufacturing method described in Claim 14 characterized by the fact that an oxidizing agent is supplied onto the surface of the aforementioned metal film to form the aforementioned oxide film.

16. The semiconductor device manufacturing method described in Claim 1 characterized by the fact that the aforementioned passive film is a film made of a material that can hinder the electrolytic reaction of the metal that constitutes the aforementioned metal film, and that the passive film is formed on the surface of the aforementioned metal film.

17. The semiconductor device manufacturing method described in Claim 16 characterized by the fact that the aforementioned passive film is a water-repellant film, an oil film, an antioxidant film, a film made of a surfactant, a film made of a chelating agent, or a film made of a silane coupling agent formed on the surface of the aforementioned metal film.

18. The semiconductor device manufacturing method described in Claim 1 characterized by the fact that the aforementioned passive film has higher electrical resistance and lower mechanical strength than the aforementioned metal film.

19. A polishing device having an electroconductive polishing tool with a polishing surface,

a polishing tool rotating and support means that supports the aforementioned polishing tool and rotates it about a prescribed axis of rotation,

a rotating and support means that supports an object to be polished and rotates it about a prescribed axis of rotation,

a positioning means that moves the aforementioned polishing tool to a target position opposite the aforementioned object to be polished,

a relative moving means that moves the polishing surface of the aforementioned polishing object relative to the polishing surface of the aforementioned polishing tool along a prescribed plane,

an electrolyte supply means that supplies an electrolyte onto the polishing surface of the aforementioned object to be polished, and

an electrolytic current supply means that, with the polishing surface of the aforementioned object to be polished used as the anode and with the aforementioned polishing

tool used as the cathode, supplies electrolytic current from the aforementioned polishing surface to the aforementioned polishing tool via the aforementioned electrolyte.

20. The polishing device described in Claim 19 further characterized by a polishing agent supply means that supplies a chemical polishing agent containing abrasive particles to the polishing surface of the aforementioned object to be polished.

21. The polishing device described in Claim 1 [sic; 19] characterized by the fact that the aforementioned electrolytic current supply means has an electricity conducting means, which is arranged in such a way that it can contact or approach the polishing surface of the aforementioned object to be polished to conduct electricity to the polishing surface with the polishing surface of the object to be polished used as an anode, and

a DC power supply that applies a prescribed voltage between the aforementioned electricity conducting means and the aforementioned polishing tool.

22. The polishing device described in Claim 21 characterized by the fact that the aforementioned DC power supply outputs a pulsed voltage with a prescribed period.

23. The polishing device described in Claim 21 characterized by the following facts: the aforementioned polishing tool has a wheel-shaped electroconductive part, an annular end surface of which forms the polishing surface;

the electricity conducting means is set away from the polishing tool on its inner side and is supported by the aforementioned rotating and support means; the electricity conducting means also has an electroconductive electrode plate that rotates together with the aforementioned polishing tool.

24. The polishing device described in Claim 23 characterized by the fact that the aforementioned electrode plate is equipped with a scrubbing part having a surface that scrubs the polishing surface on the side opposite the polishing surface of the aforementioned object to be polished.

25. The polishing device described in Claim 24 characterized by the following facts: the aforementioned scrubbing part is made of a material that can absorb the aforementioned electrolyte and the chemical polishing agent containing abrasive particles and allow them to penetrate; where the electrolyte and/or chemical polishing agent supplied from the aforementioned electrode plate side is supplied to the polishing surface of the object to be polished.

26. The polishing device described in Claim 21 characterized by the fact that the aforementioned polishing tool is supported by an electroconductive part that is connected to the aforementioned rotating and support means, and electricity is passed to the polishing tool via a conductive brush that makes contact with the aforementioned rotating electroconductive part.

27. The polishing device described in Claim 23 characterized by the fact that the aforementioned electrode part is made of a noble metal compared with the electrolyzed metal formed on the polishing surface of the aforementioned object to be polished.

28. The polishing device described in Claim 19 further characterized by a current detecting means for detecting the magnitude of the electrolytic current flowing between the polishing surface of the aforementioned object to be polished and the aforementioned polishing tool.

29. The polishing device described in Claim 23 characterized by a resistance detecting means for detecting the electrical resistance between the aforementioned electrode part and the aforementioned polishing tool via the polishing surface of the aforementioned object to be polished.

30. The polishing device described in Claim 29 characterized by further having a control means that controls the opposite positions of the aforementioned polishing tool and object to be polished based on the detected signal of the aforementioned current detecting means so that the magnitude of the aforementioned electrolytic current is kept constant.

31. A polishing device characterized by the following facts: the polishing device has a polishing tool having a polishing surface that rotates while in contact with the entire surface of the object to be polished; the polishing device rotates the aforementioned object to be polished while bringing it into contact with the aforementioned polishing surface to planarize the surface of the object to be polished;

the polishing device has an electrolyte supply means that supplies an electrolyte to the aforementioned polishing surface;

the polishing device is equipped on the aforementioned polishing surface with an anode electrode and a cathode electrode that can conduct electricity to the surface of the aforementioned object to be polished, the surface of the aforementioned object to be polished is planarized by means of composite electrolytic polishing that combines electrolytic polishing carried out with the aforementioned electrolyte and mechanical polishing carried out with the aforementioned polishing surface.

32. The polishing device described in Claim 31 characterized by the fact that the polishing device also has a polishing agent supply means that supplies a chemical polishing agent containing abrasive particles to the aforementioned polishing surface, and

the surface of the aforementioned object to be polished is planarized by means of composite electrolytic polishing that combines electrolytic polishing carried out with the aforementioned electrolyte and chemical mechanical polishing carried out with the aforementioned polishing surface and polishing agent.

33. A polishing method characterized by the following facts: the polishing surface of an electroconductive polishing tool is pressed against the surface of an object to be polished, which has a metal film formed at least on the surface or on an inner layer, with an electrolyte between them;

the aforementioned polishing tool is used as a cathode and the surface of the aforementioned object to be polished is used as an anode to supply an electrolytic current that flows from the surface of the aforementioned object to be polished to the aforementioned polishing tool via the aforementioned electrolyte;

the aforementioned polishing tool is moved relative to the object to be polished are given relative movement along a prescribed plane while in mutual rotation;

the metal film formed on the aforementioned object to be polished is planarized by means of composite electrolytic polishing that combines electrolytic polishing carried out with the aforementioned electrolyte and mechanical polishing carried out with the aforementioned polishing surface.

34. The polishing method described in Claim 33 characterized by the fact that besides the aforementioned electrolyte, there is a chemical polishing agent containing abrasive particles between the aforementioned polishing surface and the surface of the aforementioned object to be polished, and the metal film formed on the aforementioned object to be polished is planarized by means of composite electrolytic polishing that combines electrolytic polishing carried out with the aforementioned electrolyte and chemical mechanical polishing carried out with the aforementioned polishing surface and polishing agent.

35. The polishing method described in Claim 33 characterized by the following facts: multiple films made of different materials are laminated on the aforementioned object to be polished;

the electrolytic current that flows from the surface of the object to be polished to the polishing tool via the aforementioned electrolyte and that varies as a function of the difference between the electrical characteristics of the material of each of the aforementioned films is monitored; and the polishing progress is controlled based on the magnitude of the electrolytic current.

36. The polishing method described in Claim 33 characterized by the fact that a pulsed voltage with a prescribed period is applied between the aforementioned polishing tool and the surface of the aforementioned object to be polished to supply the aforementioned electrolytic current.

37. The polishing method described in Claim 33 characterized by the fact that an electrode part is brought into contact with the surface of the aforementioned object to be polished

to which the aforementioned electrolyte has been supplied or in the vicinity thereof in order to conduct electricity to the surface of the aforementioned object to be polished.

38. The polishing method described in Claim 37 characterized by the fact that the aforementioned electrode part conducts electricity to the metal film formed on the aforementioned object to be polished while it is rotated together with the aforementioned polishing tool and moved with respect to the aforementioned object to be polished.

39. The polishing method described in Claim 37 characterized by the fact that the polishing progress of the aforementioned object to be polished is controlled based on the magnitude of the electrical resistance between the aforementioned electrode part via the surface of the aforementioned object to be polished and the aforementioned polishing tool.

40. The polishing method described in Claim 34 characterized by the fact that the abrasive particles contained in the aforementioned polishing agent are positively charged.

41. A polishing method having a step in which a passive film used for hindering the electrolytic reaction of a metal film formed on an object to be polished is formed on the surface of the metal film,

a step in which the polishing surface of an electroconductive polishing tool and the metal film are pressed against each other with an electrolyte between the polishing surface and the metal film, and a prescribed voltage is applied between the aforementioned polishing tool and the aforementioned metal film,

a step in which the polishing surface of the aforementioned polishing tool and the metal film of the aforementioned object to be polished are moved relatively along a prescribed plane, and the passive film on projections of the metal film that protrude toward the polishing surface of the polishing tool are selectively removed by the electrolytic machining of the aforementioned polishing tool, and

a step in which the projections of the metal film exposed on the surface after the aforementioned passive film is removed are removed under the electrolytic polishing effect of the aforementioned electrolyte to planarize the aforementioned metal film.

42. The polishing method described in Claim 41 characterized by the fact that besides the aforementioned electrolyte, there is also a chemical polishing agent containing abrasive particles between the aforementioned polishing surface and the aforementioned metal film, and the aforementioned passive film is selectively removed by the chemical electrolytic machining carried out with the aforementioned polishing surface and abrasive particles.

43. The polishing method described in Claim 41 characterized by the fact that the aforementioned passive film is an oxide film formed by oxidizing the surface of the aforementioned metal film.

44. The polishing method described in Claim 41 characterized by the fact that the aforementioned passive film is a film made of a material that can hinder the electrolytic reaction of the metal that constitutes the aforementioned metal film, and the passive film is formed on the surface of the aforementioned metal film.

45. The polishing method described in Claim 41 characterized by the fact that the aforementioned passive film has higher electrical resistance and lower mechanical strength than the aforementioned metal film.

46. The polishing method described in Claim 41 characterized by the fact that an electrode part is brought into contact with the surface of the aforementioned metal film or in the vicinity thereof in order to conduct electricity to the aforementioned metal film.

47. The polishing method described in Claim 46 characterized by the fact that the polishing progress is controlled based on the magnitude of the electrical resistance between the aforementioned electrode part and the aforementioned polishing tool.

48. The polishing method described in Claim 42 characterized by the fact that the abrasive particles contained in the aforementioned polishing agent are positively charged.

Detailed explanation of the invention

[0001]

Technical field of the invention

The present invention pertains to a type of polishing device and a polishing method for planarization of embossed surfaces that accompany multi-layered wiring structures of semiconductor devices, as well as a manufacturing method for semiconductor devices with multi-layered wiring structure.

[0002]

Prior art

Efforts to increase integration density and miniaturization of semiconductor devices have resulted in reductions in wiring size and pitch and the development of multi-layered wiring structures. As a result, multi-layered wiring technology has become more important in the fabrication of semiconductor devices. On the other hand, the use of aluminum (Al) as the wiring material for semiconductor devices of the prior art having multi-layer wiring structures has been problematic. The recent design rule of 0.25 μm or smaller to suppress signal propagation delays has prompted extensive studies on the use of copper (Cu) in place of aluminum (Al) as the wiring material. When Cu is used as the wiring material, it is possible to realize both low electrical resistance and high resistance to electromigration, which is advantageous. For example, in the process using Cu wiring, the metal is buried in a groove-like wiring pattern previously

formed on an interlayer insulating film, and by means of CMP (Chemical Mechanical Polishing), the excess metal film is removed to form the wiring. This method, which is known as the damascene method, is a powerful wiring processing method. Because this damascene method does not require etching of the wiring, and the interlayer insulating film applied thereon is self-planarizing, the operation is simple. This [simplicity] is a characteristic feature of this method. In addition, there is the dual damascene method, in which in addition to wiring on the interlayer insulating film, contact holes are also formed as grooves, wiring and contact holes are buried with metal at the same time. This method can further simplify the wiring operation significantly.

[0003]

In the following, an example of the wiring formation process using said dual damascene method will be explained with reference to Figures 32-37. Also, the case when Cu is used as the wiring material will also be explained. First, as shown in Figure 32, for example, on substrate (301) made of silicon or another semiconductor material having impurity diffusion regions (not shown in the figure) formed on it appropriately, interlayer insulating film (302) made of, e.g., silicon oxide film, is formed using, e.g., reduced-pressure CVD (Chemical Vapor Deposition). Then, as shown in Figure 33, grooves (304) where wiring is formed with a prescribed pattern is formed and electrically connected to contact holes (303), which pass through impurity diffusion regions of substrate (301), and impurity diffusion regions of substrate (301) by means of the conventional photolithographic technology and etching technology. Then, as shown in Figure 34, barrier film (305) is formed on the surface of interlayer insulating film (302) and inside contact holes (303) and grooves (304). This barrier film (305) is formed from Ta, Ti, TaN, TiN, or another material using conventional sputtering techniques. Barrier film (305) is formed to prevent the material that forms the wiring from diffusing into interlayer insulating film (302). In particular, when Cu is used as the wiring material and silicon oxide film is used as interlayer insulating film (302), because Cu has a high diffusion coefficient into silicon oxide film and tends toward oxidation, measures should be taken to prevent problems from taking place.

[0004]

Then, as shown in Figure 35, seed Cu film (306) is formed with a prescribed film thickness on barrier film (305) by means of the conventional sputtering method. Then, as shown in Figure 36, Cu film (307) is formed such that contact holes (303) and grooves (304) are filled with Cu. For example, Cu film (307) may be formed using a plating method, CVD method, sputtering method, or the like. Then, as shown in Figure 37, interlayer insulating film (302) is planarized by removing excess Cu film (307) and barrier film (305) using the CMP method. In

this way, wiring (308) and contact [holes] (309) are formed. By repeating the aforementioned process on wiring (308), it is possible to obtain a multi-layered wiring structure.

[0005]

Problems to be solved by the invention

However, the use of the dual damascene method to form the aforementioned multi-layered wiring is also problematic. In the step of removal of excess Cu film (307) and barrier film (305) using CMP method, the difference in the removal rates of interlayer insulating film (302), Cu film (307), and barrier film (305) easily produces dishing, erosion (thinning), recesses, etc., which is undesirable. As shown in Figure 38, dishing refers to the formation of a hollow in the central wiring portion due to excess removal of wiring when there exists wiring (308) with widths as large as, e.g., about 100 μm with respect to a design rule of about 0.18- μm . When said dishing takes place, the cross-sectional area of wiring (308) becomes insufficient, so that problems take place with the wiring resistance, etc. Dishing is likely to occur when copper, aluminum, or another soft material is used as the wiring material. As shown in Figure 39, erosion refers to the phenomenon of excess removal of the portion with a higher pattern density where wiring with a width of, e.g., 1.0 μm is formed at a density of 50% in a range of about 3000 μm . When erosion takes place, the cross-sectional area of the wiring becomes insufficient, so that problems occur with the wiring resistance, etc. As shown in Figure 40, recesses refers to the phenomenon of the formation of steps as wiring (308) becomes lower at the boundary between interlayer insulating film (302) and wiring (308). Here, too, because the cross-sectional area of the wiring is insufficient, problems take place with the wiring resistance, etc. In addition, in the step of removal of excess Cu film (307) and barrier film (305) using CMP, it is necessary to remove Cu film (307) and barrier film (305) with great efficiency, and the polishing rate, that is, the amount removed per unit time, should be higher than, e.g., 500 nm/min. In order to realize this polishing rate, the pressure applied to the wafer must be increased. However, as the processing pressure is increased, as shown in Figure 41, the wiring surface is prone to scratches SC and chemical damage CD. In particular, these problems may readily occur with Cu and aluminum, since they are soft. Consequently, these problems are the source of open circuits, short circuits, poor wiring resistance, and other defects. Also, as the processing pressure is increased, said problems of dishing, erosion, and recesses become exacerbated, which is undesirable.

[0006]

The purpose of the present invention is to solve the aforementioned problems of the conventional methods by providing a polishing apparatus and polishing method as well as a

semiconductor device manufacturing method characterized by the fact that when wiring or other metal film of a semiconductor device having a multi-layered wiring structure is polished for planarization, the initial bumps and dips can be easily planarized, removal of the excess metal film can be performed at a high efficiency, and it is possible to suppress problems of dishing, erosion, etc. with excess removal of metal film.

[0007]

Means to solve the problems

The present invention provides a polishing apparatus characterized by the fact that it has the following parts: an electroconductive polishing tool with a polishing surface; a polishing tool rotating and supporting means that supports the aforementioned polishing tool and rotates it about a prescribed axis of rotation; a rotating and supporting means that supports a workpiece and rotates it about a prescribed axis of rotation; a moving and positioning means that moves the aforementioned polishing tool to a target position in the direction opposite to the aforementioned workpiece; a relative movement means that moves the polishing surface of the aforementioned workpiece relative to the polishing surface of the aforementioned polishing tool along a prescribed plane; an electrolyte supply means that supplies an electrolyte to the polishing surface of the aforementioned workpiece; and an electrolytic current supply means, which, with the polishing surface of the aforementioned workpiece used as the anode and the aforementioned polishing tool as the cathode, supplies electrolytic current from the aforementioned polishing surface of the workpiece to the aforementioned polishing tool via the aforementioned electrolyte.

[0008]

Also, the polishing apparatus of the present invention has a polishing tool that has a polishing surface which rotates while in contact with the entire workpiece surface to be polished; the polishing apparatus rotates the aforementioned workpiece while bringing it in contact with the aforementioned polishing surface to planarize the surface of the workpiece; the polishing apparatus has an electrolyte supply means that supplies an electrolyte onto the aforementioned polishing surface; on the aforementioned polishing surface, the polishing apparatus is equipped with an anode electrode and a cathode electrode that can conduct electricity to the surface to be polished of the aforementioned workpiece; the surface of the aforementioned workpiece is planarized by means of composite electrolytic polishing that combines electrolytic polishing carried out with the aforementioned electrolyte and mechanical polishing carried out with the aforementioned polishing surface.

[0009]

The present invention also provides a polishing method characterized by the following facts: the polishing surface of an electroconductive polishing tool is pressed against the surface of the workpiece, which has a metal film formed at least on the surface or on an inner layer, with an electrolyte between them; the aforementioned polishing tool is used as the cathode and the surface of the aforementioned workpiece is used as the anode to supply an electrolytic current that flows from the surface of the aforementioned workpiece to the aforementioned polishing tool via the aforementioned electrolyte; the aforementioned polishing tool and workpiece are moved relatively toward one another along a prescribed plane while being jointly rotated; the metal film formed on the aforementioned workpiece is planarized by means of composite electrolytic polishing that combines electrolytic polishing carried out with the aforementioned electrolyte and mechanical polishing carried out with the aforementioned polishing surface.

[0010]

Also, the present invention provides a polishing method comprising the following steps: a step in which a passive film used to hinder the electrolytic reaction of a metal film formed on a workpiece is formed on the surface of the metal film; a step in which the polishing surface of an electroconductive polishing tool and the metal film are pressed against each other with an electrolyte between the polishing surface and the metal film, and a prescribed voltage is applied between the aforementioned polishing tool and the aforementioned metal film; a step in which the polishing surface of the aforementioned polishing tool and the metal film of the aforementioned workpiece are driven to move relatively toward one another along a prescribed plane, and the passive film on the bumps of the metal film that protrude towards the polishing surface of the polishing tool are selectively removed as a result of the mechanical polishing of the aforementioned polishing tool; and a step in which the aforementioned passive film is removed, and bumps of the metal film exposed on the surface after removal of the aforementioned passive film are removed under the electrolytic polishing effect of the aforementioned electrolyte to planarize the aforementioned metal film.

[0011]

The present invention also provides a semiconductor device manufacturing method characterized by the fact that it comprises the following steps: a step in which wiring grooves used for forming wiring are formed on an insulating film formed on a substrate; a step in which a metal film is deposited on the aforementioned insulating film to bury the aforementioned wiring grooves; a step in which a passive film for hindering the electrolytic reaction of the metal film is formed on the surface of the metal film deposited on the aforementioned insulating film; a step in

which the portions of the passive film on bumps existing on the surface of the aforementioned metal film due to burying the aforementioned wiring grooves are selectively removed by means of mechanical polishing to expose bumps of the metal to the surface; and a step in which the exposed bumps of the aforementioned metal film are removed by means of electrolytic polishing to planarize bumps and dips formed on the surface of the aforementioned metal film due to burying of the aforementioned wiring grooves.

[0012]

Also, the semiconductor device manufacturing method of the present invention has a step in which the excess metal film existing on the insulating film of the aforementioned surfaced metal film is removed by means of composite electrolytic polishing that combines electrolytic polishing and mechanical polishing to form the aforementioned wiring.

[0013]

In the semiconductor device manufacturing method of the present invention, a passive film is formed on the metal film having bumps and dips on its surface, and the passive film is then removed mechanically. In this way, the bumps of the metal film are exposed to the surface. With the remaining passive film used as a mask, electrolysis is performed by means of an electrolyte so as to selectively remove the bumps of the metal film. As a result, the initial bumps and dips on the metal film are removed and the metal film is planarized. Also, with the initial bumps and dips of the metal film planarized, the excess metal film existing on the insulating film during the formation of wiring is removed with great efficiency by means of electrolytic composite polishing. After the excess metal film is removed and the insulating film is exposed, the electrolysis operation for this portion is stopped automatically, and the metal film buried in the wiring grooves formed on the insulating film is not removed as excess metal film.

[0014]

Embodiment of the invention

In the following, an embodiment of the present invention will be explained with reference to figures.

Constitution of the polishing apparatus

Figure 1 is a diagram illustrating the constitution of the polishing apparatus in an embodiment of the present invention. Figure 2 is an enlarged view of the main portion of the processing head unit of the polishing apparatus shown in Figure 1. As shown in Figure 1, polishing apparatus (1) has processing head unit (2), electrolysis power source (61), controller

(55) that controls the entire system of polishing apparatus (1), slurry feeder (71), and electrolyte feeder (81). Also, although not shown in the figure, polishing apparatus (1) is set in a clean room. There is a transporting port for transporting a wafer cassette with a wafer as the workpiece to be polished contained in it into/from the aforementioned clean room. In addition, a wafer transporting robot is arranged between transporting port and polishing apparatus (1) for transferring the wafer between the wafer cassette, which has been transported into the clean room through the transporting port, and polishing apparatus (1).

[0015]

Processing head unit (2) has polishing tool support unit (11) that supports and rotates polishing tool (3) and supports polishing tool (3) [sic], Z-axis positioning mechanism (31) that positions polishing tool support unit (11) at the target position in the Z-axis direction, and X-axis moving mechanism (41) that supports and rotates wafer W as the workpiece and moves it in the X-axis direction. In this case, polishing tool support unit (11) corresponds to an example of the polishing tool rotating/supporting means of the present invention; X-axis moving mechanism (41) corresponds to an example of the rotating/supporting means and relative movement means of the present invention; and Z-axis positioning mechanism (31) corresponds to an example of the moving/positioning means of the present invention.

[0016]

Z-axis positioning mechanism (31) has Z-axis servomotor (18) that is fixed on a column not shown in the figure, Z-axis slider (16) that is connected to supporting device (12) and principal shaft motor (13) and has a threaded portion for ball screw shaft (18a) connected to Z-axis servomotor (18), and guide rail (17) arranged on a column (not shown in the figure) that supports Z-axis slider (16) to enable its free movement in the Z-axis direction.

[0017]

Z-axis servomotor (18) is rotationally driven by drive current from Z-axis driver (52) connected to Z-axis servomotor (18). Ball screw shaft (18a) is arranged along the Z-axis direction. One end of the ball screw shaft is connected to Z-axis servomotor (18), and the other end is supported in a freely rotatable manner by a supporting member set on said column (not shown in the figure). In this way, Z-axis positioning mechanism (31) positions polishing tool (3) supported by polishing tool support unit (11) to any position in the Z-axis direction via Z-axis servomotor (18). For example, the positioning precision of Z-axis positioning mechanism (31) corresponds to a resolution of about 0.1 μm .

[0018]

X-axis moving mechanism (41) has wafer table (42) that chucks wafer W, supporting device (45) that supports wafer table (42) in a freely rotatable manner, drive motor (44) that supplies torque to rotate wafer table (42), belt (46) that connects drive motor (44) and the rotating shaft of supporting device (45), processing pan (47) set on supporting device (45), X-axis slider (48) that has drive motor (44) and supporting device (45) arranged thereon, X-axis servomotor (49) supported on a frame (not shown in the figure), ball screw shaft (49a) connected to X-axis servomotor (49), and movable member (49b) that has a threaded portion for ball screw shaft (49a) connected to X-axis slider (48).

[0019]

Wafer W is held on wafer table (42) by means of a vacuum pump, e.g. processing pan (47) is used to recover used electrolyte, slurry, or other liquids. Drive motor (44) is driven by the drive current from table driver (53). By controlling this drive current, one can rotate wafer table (42) at a prescribed rotational velocity. X-axis servomotor (49) is driven to rotate by the drive current fed from X-axis driver (54) connected to X-axis servomotor (49), and X-axis slider (48) is driven in the X-axis direction via ball screw shaft (49a) and movable member (49b). In this case, by controlling the drive current fed to X-axis servomotor (49), one can control the velocity of wafer table (42) in the X-axis direction.

[0020]

Figure 2 is a diagram illustrating an example of the internal structure of polishing tool support unit (11). Polishing tool support unit (11) has polishing tool (3), flange member (4) for supporting polishing tool (3), supporting device (12) for supporting flange member (4) in a freely rotatable manner, principal shaft motor (13) that is connected to principal shaft (12a) supported by supporting device (12) and rotates said principal shaft (12a), and cylinder device (14) arranged on principal shaft motor (13).

[0021]

For example, principal shaft motor (13) is a direct drive motor. The rotor (not shown in the figure) of the direct drive motor is connected to principal shaft (12a) supported by supporting device (12). Also, principal shaft motor (13) has a through-hole at its central portion for inserting piston rod (14b) of cylinder device (14). Principal shaft motor (13) is driven by drive current fed from principal shaft driver (51).

[0022]

Supporting device (12) contains an air bearing, e.g. By means of the air bearing, principal shaft (12a) is supported in a freely rotatable manner. Principal shaft (12a) of supporting device (12) also has a through-hole at its central portion for inserting piston rod (14b) of cylinder device (14).

[0023]

Flange member (4) is made of metal. It is connected to principal shaft (12a) of supporting device (12). It has opening portion (4a) at the bottom, and polishing tool (3) is attached to its lower end surface (4b). Upper end surface (4c) of flange member (4) is connected to prussic acid (12a) supported with supporting device (12), and, as principal shaft (12a) rotates, flange member (4) also rotates. Upper end surface (4c) of flange member (4) is in contact with conducting brush (27) fixed on electroconductive conductor (28) arranged on the side surface of principal shaft motor (13) and supporting device (12), so that an electrical connection is formed between conducting brush (27) and flange member (4).

[0024]

Cylinder device (14) is fixed on the housing principal shaft motor (13). It contains piston (14a). Piston (14a) can be driven in either direction A1 or direction A2 under pneumatic force fed to cylinder device (14). Piston rod (14b) is connected to said piston (14a). Piston rod (14b) goes through the center of principal shaft motor (13) and supporting device (12) and protrudes from opening portion (4a) of flange member (4). Pressing member (21) is connected to the tip of piston rod (14b). This pressing member (21) is connected by means of a connecting mechanism that allows a change in orientation over a prescribed range with respect to piston rod (14b). Pressing member (21) can make contact with the peripheral portion of opening (22a) of insulating plate (22) arranged at the opposite position, and as piston rod (14b) is driven to move in direction A2, it presses against insulating plate (22).

[0025]

A through-hole is formed at the central portion of piston rod (14b) of cylinder device (14). Conducting shaft (20) is inserted in the through-hole, and it is fixed with respect to piston rod (14b). Conducting shaft (20) is made of an electroconductive material. Its upper end passes through piston (14a) of cylinder device (14) and extends to rotary joint (15) arranged on cylinder device (14). Its lower end passes through piston rod (14b) and pressing member (21) to reach electrode plate (23), and it is connected to electrode plate (23).

[0026]

A through-hole is formed at the central portion of conducting shaft (20), and this through-hole forms a feeding nozzle for feeding a chemical polishing agent (slurry) and electrolyte onto wafer W. Also, conducting shaft (20) has the function of forming an electrical connection between rotary joint (15) and electrode plate (23).

[0027]

Rotary joint (15) connected to the upper end portion of conducting shaft (20) is electrically connected to the positive electrode of electrolytic electrode (61), and this rotary joint (15) maintains a supply of power to conducting shaft (20) even as conducting shaft (20) rotates. That is, even while conducting shaft (20) rotates, a positive potential is still applied from electrolytic electrode (61) by means of rotary joint (15).

[0028]

Electrode plate (23) connected to the lower end of conducting shaft (20) is made of a metal, in particular, a metal more noble than that of the metal film formed on wafer W. The upper side of electrode plate (23) is supported by insulating plate (22), the outer peripheral portion of electrode plate (23) is fitted to insulating plate (22), and its lower side has smoothing element (24) bonded to it.

[0029]

Figure 3(a) is a bottom view illustrating an example of the structure of electrode plate (23). Figure 3(b) is a cross-sectional view illustrating the positional relationship of electrode plate (23), conducting shaft (20), smoothing element (24) and insulating member (4). As shown in Figure 3(a), circular opening portion (23a) is formed at the central portion of electrode plate (23). With said opening portion (23a) at the center, multiple grooves (23b) are formed extending in the radial direction of electrode plate (23). Also, as shown in Figure 3(b), the lower end portion of conducting shaft (20) is fitted and fixed on opening portion (23a) of electrode plate (23). By means of this constitution, slurry and electrolyte fed through feeding nozzle (20a) formed at the central portion of conducting shaft (20) pass through grooves (23b) and are spread over the entire surface of smoothing element (24). That is, while electrode plate (23), conducting shaft (20), smoothing element (24) and insulating member (4) are rotated, slurry and electrolyte pass through feeding nozzle (20a) formed at the central portion of conducting shaft (20) and are fed onto the upper surface of smoothing element (24), so that the slurry and electrolyte are spread over the entire upper surface of smoothing element (24). Also, smoothing element (24) and feeding nozzle (20a) of conducting shaft (20) correspond to the polishing agent feeding

means and electrolyte feeding means of the present invention, respectively. Also, electrode plate (23), conducting shaft (20) and rotary joint (15) correspond to the conducting means of the present invention.

[0030]

Smoothing element (24) bonded to the lower surface of electrode plate (23) is made of a material that can absorb electrolyte and slurry and allow them pass to the upper surface and lower surface. Also, the surface of said smoothing element (24) that faces wafer W is the surface that is in contact with wafer W and scrubs wafer W. It may be made of a soft brush-like material, spongy material, porous material, or another material that does not cause scratches, etc. on the surface of wafer W. For example, it may be made of a porous material, such as urethane resin, melamine resin, epoxy resin, polyvinyl acetal (PVA), or another resin.

[0031]

Insulating plate (22) is made of a ceramic or another insulating material. This insulating plate (22) is connected to principal shaft (12a) of supporting device (12) by means of multiple rod-shaped connecting members (26). Said connecting members (26) are set equidistantly with a prescribed radius from the center of insulating plate (22), and they are supported to move freely with respect to principal shaft (12a) of supporting device (12). Consequently, insulating plate (22) can move in the axial direction of principal shaft (12a). Also, insulating plate (22) and principal shaft (12a) are connected to each other by means of elastic members (25), such as coil springs or the like, corresponding to connecting members (26).

[0032]

Insulating plate (22) has a constitution in which it can move freely with respect to principal shaft (12a) of supporting device (12), and insulating plate (22) and principal shaft (12a) are connected to each other by means of elastic member (25). In this way, when highly compressed air is fed to cylinder device (14) so that piston rod (14b) descends in direction A2, pressing member (21) pushes insulating plate (22) downward against the recovering force of elastic member (25). In this process, smoothing element (24) also descends. In this state, if feeding of the highly compressed air to cylinder device (14) is stopped, under the recovering force of elastic member (25), insulating plate (22) rises, and smoothing element (24) rises together with it.

[0033]

Polishing tool (3) is fixed on annular lower end surface (4b) of flange member (4). This polishing tool (3) has the form of a in wheel shape, with annular polishing surface (3a) equipped on its lower end surface. Polishing tool (3) is made of an electroconductive material, which is preferably relatively soft. For example, it may be made of a material with the binder matrix (binding agent) itself electroconductive, such as carbon or a porous material made of urethane resin, melamine resin, epoxy resin, polyvinyl acetal (PVA) resin, or another resin containing sintered copper, metal compound, or other electroconductive material. Polishing tool (3) is directly connected to flange member (4) made of a porous material, and power is fed to it from conducting brush (27) that is in contact with flange member (4). That is, electroconductive conducting member (28) arranged on the side surface of principal shaft motor (13) and supporting device (12) is electrically connected to the negative electrode of electrolysis power source (61). Conducting brush (27) arranged on conducting member (28) is in contact with upper end surface (4c) of flange member (4). In this way, polishing tool (3) is electrically connected to electrolysis power source (61) through conducting member (28), conducting brush (27) and flange member (4).

[0034]

For example, as shown in Figure 4, polishing surface (3a) of polishing tool (3) is inclined at a small angle with respect to the central axis. Also, principal shaft (12a) of supporting member (12) is also inclined with respect to the principal surface of wafer W at the same inclination as polishing surface (3a). For example, one may effect a small inclination of principal shaft (12a) by adjusting the orientation with which supporting member (12) is mounted on Z-axis slider (16). In this way, since the central shaft of polishing tool (3) is inclined at a small angle with respect to the principal surface of wafer W, when polishing surface (3a) of polishing tool (3) is pressed against wafer W under a prescribed processing force F, the effective functional region S of polishing surface (3a) with respect to wafer W becomes a linear region extending in the radial direction of polishing tool (3), as shown in Figure 4. Consequently, when wafer W is driven to move in the X-axis direction towards polishing tool (3) and polishing in this direction is carried out, the effective surface area S remains almost constant, as can be seen from Figures 5a and 5b. In the present embodiment, polishing apparatus (1) has a portion of polishing surface (3a) of polishing tool (3) that acts partially on the surface of wafer W, and the effective functional area S is moved uniformly over the surface of wafer W, so that the entire surface of wafer W is polished uniformly.

[0035]

Electrolysis power source (61) is a device that applies a prescribed voltage between said rotary joint (15) and conducting brush (12). As a voltage is applied between rotary joint (15) and conducting brush (12), a potential difference takes place between polishing tool (3) and smoothing element (24). Instead of a contact-voltage power source that outputs a contact voltage at all times, electrolysis power source (61) is preferably a DC power source that contains a switching regulator circuit for outputting voltage pulses with a prescribed period. More specifically, it may be a power source that outputs voltage pulses with a prescribed period, with the pulse width appropriately adjustable. As an example, the output voltage may be 150 VDC, the maximum output current may be 2-3 A, and the pulse width may be adjusted to any of the values 1, 2, 5, 10, 20 and 50 μ s. Since said voltage pulses with the aforementioned short pulse width are output, the electrolysis eluting amount for each pulse is very small. That is, this method can effectively prevent or minimize large crater-shaped eruption elution of the metal film caused by a discharge in an abrupt change of the inter-electrode distance when contact is made with bumps and dips of the metal film formed on the surface of wafer W or by spark discharge or the like due to abrupt changes in the electrical resistance when gas bubbles, particles, etc. are included. Also, as the output voltage is relatively high as compared with the output current, one can have a certain margin in setting the inter-electrode distance. That is, even when the inter-electrode distance undergoes a certain change, there is still little change in the current, because the output voltage is high.

[0036]

Electrolysis power source (61) has ammeter (62) as the current detecting means of the present invention. This ammeter (62) is set for monitoring the electrolytic current flowing in electrolysis power source (61), and the monitored current signal (62s) is output to controller (55). Also, electrolysis power source (61) has resistance meter (63) as the resistance detecting means of the present invention. This resistance meter (63) is arranged to monitor the electrical resistance between polishing tool (3) and electrode plate (23) via the surface of wafer W on the basis of the current from electrolysis power source (61). The monitored electrical resistance signal (63s) is output to controller (55).

[0037]

Slurry feeder (71) feeds slurry to feeding nozzle (20a) of said conducting shaft (20). The slurry for polishing metals may be used in this case, such as the slurry prepared by containing aluminum oxide (alumina), cerium oxide, silica, germanium oxide, etc. as abrasive particles in an oxidative aqueous solution based on hydrogen peroxide, iron nitrate, potassium iodate, or the

like. Also, the abrasive particles are pre-charged positively so as to maintain the colloidal state with good dispersability.

[0038]

Electrolyte feeder (81) feeds electrolyte EL to processing head unit (11). Electrolyte EL is a solution made of a solvent and an ionically separated solute. For example, the electrolyte may be made of an aqueous solution prepared by adding a reducing agent to a system of nitrate or chloride.

[0039]

Controller (55) has the function of controlling the entirety of polishing apparatus (1). More specifically, control signal (51s) is output to principal shaft driver (51) to control the rotational velocity of polishing tool (3). Control signal (52s) is output to Z-axis driver (52) to perform positioning control of polishing tool (3) in the Z-axis direction. Control signal (53s) is output to table driver (53) to control the rotational velocity of wafer W. Control signal (54s) is output to X-axis driver (54) to control the velocity of wafer W in the X-axis direction. Also, controller (55) controls the operation of electrolyte feeder (81) and slurry feeder (71), as well as feeding of electrolyte EL and slurry SL to processing head unit (2).

[0040]

Also, controller (55) can control the output voltage, output pulse frequency, and output pulse width, etc. of electrolysis power source (61). Also, current signal (62s) and electrical resistance signal (63s) are input to controller (55) from ammeter (62) and resistance meter (63) of electrolysis power source (61). Based on said current signal (62s) and electrical resistance signal (63s), controller (55) can control the operation of polishing apparatus (1). More specifically, in order to produce a contact electrolytic current from current signal (62s), current signal (62s) is used as a feedback signal for controlling Z-axis servomotor (18), and, based on the current and electrical resistance defined by current signal (62s) and electrical resistance (63s), the polishing processing is stopped, as operation of polishing apparatus (1) is controlled.

[0041]

The operator inputs various data to control panel (56) connected to controller (55), and for example, monitored current signal (62s) and electrical resistance signal (63s) are displayed.

[0042]

In the following, the polishing operation of said polishing apparatus (1) will be explained with reference to an example of polishing of a metal film formed on the surface of wafer W. Also, the case when a metal film of copper is formed will be explained. First of all, wafer W is chucked on wafer table (45), and wafer table (45) is driven to rotate wafer W at a prescribed rotational velocity. Also, wafer table (45) is driven to move in X-axis direction, so that polishing tool (3) mounted on flange portion (4) is positioned at a prescribed site above wafer W, and polishing tool (3) is rotated at a prescribed rotational velocity. When polishing tool (3) is rotated, insulating plate (22), electrode plate (23) and smoothing element (24) connected to flange portion (4) are also driven to rotate. Also, pressing member (21) that presses smoothing element (24), piston rod (14b), piston (14a), and conducting shaft (20) are also rotated at the same time.

[0043]

In this state, when slurry SL and electrolyte EL are fed from slurry feeder (71) and electrolyte feeder (81), respectively, to feeding nozzle (20a) inside conducting shaft (20), slurry SL and electrolyte EL are fed over the entire surface of smoothing element (24). Polishing tool (3) is lowered in the Z-axis direction so that polishing surface (3a) of polishing tool (3) comes in contact with the surface of wafer W, and a prescribed processing pressure is applied. Also, when electrolysis power source (61) is turned on, a negative potential is applied via conducting brush (27) to polishing tool (3), and a positive potential is applied via rotary joint (15) to smoothing element (24).

[0044]

In addition, since highly compressed air is fed to cylinder device (14), piston rod (14b) is lowered in direction A2 shown in Figure 1, and the lower surface of smoothing element (24) is driven to move to a position where it is in contact with or near wafer W. In this state, wafer table (45) is driven to move in the X-axis direction with a prescribed velocity pattern, so that the entire surface of wafer W is uniformly polished during the processing.

[0045]

Figure 6 is a schematic diagram illustrating the state in which polishing tool (3) in polishing apparatus (1) is lowered in the Z-axis direction to make contact with the surface of wafer W. Figure 7 is an enlarged view inside circle C of Figure 6. Figure 8 is an enlarged diagram illustrating the portion inside circle D of Figure 7. As shown in Figure 7, smoothing element (24) is set via electrolyte EL fed onto wafer W or directly on metal film MT formed on wafer W, so that power is fed to it as the anode, and polishing tool (3) is also set either via

electrolyte EL supplied to wafer W or directly on metal film MT formed on wafer W, and power is fed to it as the cathode. Also, as shown in Figure 7, there is a gap Γ_b between metal film MT and smoothing element (24). In addition, as shown in Figure 8, there is a gap Γ_w between metal film MT and polishing surface (3a) of polishing tool (3). As shown in Figure 7, insulating plate (4) is included between polishing tool (3) and smoothing element (24) (electrode plate (23)). Since resistance R_0 of insulating plate (4) is very high, current i_0 flowing from smoothing element (24) via insulating plate (4) to polishing tool (3) is almost zero, and there is no current flowing from smoothing element (24) via insulating plate (4) to polishing tool (3).

[0046]

Consequently, the current from smoothing element (24) to polishing tool (3) is split into current i_1 flowing directly via resistance R_1 in electrolyte EL to polishing tool (3) and current i_2 flowing in polishing tool (3) from electrolyte EL and via metal film MT of copper formed on the surface of wafer W, then through electrolyte EL again and to polishing tool (3). Since current i_2 flows to the surface of metal film MT, copper that forms metal film MT is ionized and eluted into electrolyte EL due to the electrolytic function of electrolyte EL.

[0047]

In this case, resistance R_1 of electrolyte EL becomes very high in proportion to distance d between smoothing element (24) as the anode and polishing tool (3) as the cathode. Consequently, by selecting an inter-electrode distance d to be sufficiently larger than the gap Γ_b and the gap Γ_w , current i_1 flowing directly via resistance R_1 in electrolyte EL to polishing tool (3) is very low, and current i_2 becomes high, so that almost all of the electrolytic current flows through the surface of metal film MT. Consequently, it is possible to perform electrolytic elution of copper that forms metal film MT highly efficiently. Also, the magnitude of current i_2 can be changed as a function of the gaps Γ_b and Γ_w . Consequently, as explained above, by adjusting the magnitude of gaps Γ_b and Γ_w by controlling the position of polishing tool (3) in Z-axis using controller (55), one can have a contact value for current i_2 . Adjustment of the magnitude of gap Γ_w can be carried out by controlling Z-axis servomotor (18) with current signal (62s) used as a feedback signal such that the electrolytic current obtained from current signal (62s), that is, current i_2 , is contact. Also, the precision in positioning polishing apparatus (1) in the Z-axis direction is as high as corresponding to a resolution of $0.1 \text{ }\Gamma_m$. Also, as principal shaft (12a) is inclined at a small angle with respect to the principal surface of wafer W, contact area S is always held constant during the process. Consequently, by controlling the electrolytic current to a constant level, one always has a contact current density, and thus a contact electrolysis elution rate of the metal film.

[0048]

As explained above, for polishing apparatus (1) with the aforementioned constitution, it has an electrolytic polishing function for eluting and removing metal film MT formed on said wafer W due to the electrolytic function of electrolyte EL. In addition to the electrolytic polishing function, polishing apparatus (1) with the aforementioned constitution also has the chemical mechanical polishing function of the conventional CMP apparatus by means of polishing tool (3) and slurry SL, and it is possible to polish wafer W by means of a composite function of the aforementioned electrolytic polishing function and chemical mechanical polishing (hereinafter referred to as electrolytic composite polishing). Also, polishing apparatus (1) with the aforementioned constitution may perform the polishing processing by means of the composite function of the mechanical polishing and electrolytic polishing function using polishing surface (3a) of polishing tool (3), without using slurry SL. Because polishing apparatus (1) can polish the metal film by means of the composite function of electrolytic polishing and chemical mechanical polishing, it is possible to remove the metal film with an efficiency much higher than that of the polishing apparatus that makes use of only chemical mechanical polishing or mechanical polishing. Because a high polishing rate can be realized for the metal film, it is possible to reduce processing force F applied by polishing tool (3) to wafer W as compared with that of the polishing apparatus that makes use of only chemical mechanical polishing or mechanical polishing, and it is possible to suppress dishing or erosion.

[0049]

The polishing method using the electrolytic composite polishing function of polishing apparatus (1) in another embodiment will be explained below with reference to an example when this method is applied in the wiring forming process using the dual damascene method for a semiconductor device having a multi-layered wiring structure.

[0050]

Figure 9 is a diagram illustrating the manufacturing process in an embodiment of the semiconductor device manufacturing method of the present invention. In the following, the manufacturing process of the present embodiment will be examined on the basis of the flow chart of Figure 9. First, as shown in Figure 10, on wafer W made of silicon or other semiconductor and having impurity diffusion regions (not shown in the figure) suitably formed thereon, interlayer insulating layer (102) made of silicon oxide film (SiO_2) is formed using reduced-pressure CVD (Chemical Vapor Deposition) with, e.g., TEOS (tetraethyl orthosilicate) used as the reaction source. Then, as shown in Figure 11, contact holes (103) through impurity

diffusion region of the wafer and wiring grooves (104) where wiring of a prescribed pattern for forming electrical connections to the impurity diffusion region of wafer W are formed using the conventional photolithographic technology and etching technology. Also, the depth of wiring grooves (104) is about 800 nm.

[0051]

Then, as shown in Figure 12, barrier film (105) is formed on the surface of interlayer insulating film (102) and inside contact holes (103) and wiring grooves (104). Said barrier film (305) may be formed from Ta, Ti, TaN, TiN or another material with a film thickness of about 15 nm using a sputtering apparatus, vacuum vapor deposition apparatus, etc. Barrier film (305) is used to prevent the material that forms the wiring from diffusing into interlayer insulating film (102), and for improving adhesion to interlayer insulating film (102). In particular, when copper is used as the wiring material and silicon oxide film is used as interlayer insulating film (102), because copper has a high diffusion coefficient with respect to the silicon oxide film and tends toward oxidation, this problem should be prevented. The aforementioned process is process PR1 shown in Figure 9.

[0052]

Then, as shown in Figure 13, seed film (106) made of the same material as the wiring forming material, such as copper, is formed to a thickness of about 150 nm on barrier film (105) using the conventional sputtering method (process PR2). Seed film (106) is used to promote the growth of copper grains when copper is buried in wiring grooves and contact holes. Then, as shown in Figure 14, metal film (107) with a thickness of about 2000 nm and made of copper is formed on barrier film (105) such that it fills contact holes (103) and wiring grooves (104). It is preferred that metal film (107) be formed using an electroplating or non-electroplating technique. However, it is also possible to form it using a CVD method, sputtering method, etc. Also, seed film (106) is integrated with metal film (107) (process PR3).

[0053]

Figure 15 is an enlarged cross-sectional view of the semiconductor device midway during the manufacturing process with metal film (107) formed on barrier film (105). As can be seen from Figure 15, because contact holes (103) and wiring grooves (104) are buried, 600-nm bumps and dips are formed. Although the aforementioned operation is performed in the same way as in the conventional process, in the polishing method of the present invention, excess metal film (107) and barrier film (105) on interlayer insulating film (102) are removed by means of an electrolytic composite polishing operation using said polishing apparatus (1), instead of chemical

mechanical polishing. Also, in the polishing method of the present invention, as shown in Figure 16, passive film (108) is formed on the surface of metal film (107) before the aforementioned process of electrolytic composite polishing (process PR4). This passive film (108) is made of a material that can hinder the electrolytic reaction of the metal (copper) that forms metal film (107).

[0054]

As far as the formation method of passive film (108) is concerned, for example, an oxidizing agent may be coated on the surface of metal film (107) to form an oxide film. When copper is used as the metal for forming metal film (107), copper oxide (CuO) film is formed as the passive film. As another method, passive film (108) may be formed as a water-repellant film, oil film, oxidation inhibiting film, a film made of a surfactant, a film made of chelating agent, or a film made of a silane coupling agent on the surface of metal film (107). There is no particular limitation on the type of passive film (108). However, it is preferred that the material of the passive film (108) have an electrical resistance greater than that of metal film (107), and that the material have a relatively low mechanical strength and be brittle.

[0055]

Then, in the polishing method of the present invention, passive film (108) formed only on bumps of metal film (107) is selectively removed (process PR5). Selective removal of passive film (108) is carried out using said polishing apparatus (1). Also, a slurry having a high polishing rate for copper is used as slurry SL. Examples of slurries that may be used include those prepared by adding alumina-, silica-, or manganese-based abrasive particles in an aqueous solution based on hydrogen peroxide, iron nitrate, potassium iodate, etc. First, wafer W is clamped on wafer table (42) of polishing apparatus (1). While electrolyte EL and slurry SL are fed onto wafer W, rotating polishing tool (3) and smoothing element (24) are lowered in the Z-axis direction to make contact with or approach wafer W. Then, wafer W is driven to move at a prescribed velocity pattern in the X-axis direction for polishing processing. With polishing tool (3) used as the negative electrode and electrode plate (23) as the positive electrode, pulsed DC voltage is applied between polishing tool (3) and electrode plate (23). Also, by having the aqueous solution for preparing slurry SL take on the function of electrolyte SL [sic; EL], it is also possible to feed only slurry SL onto wafer W.

[0056]

Figure 17 is a schematic diagram illustrating the polishing process near smoothing element (24) in the aforementioned state. Figure 18 is a schematic diagram illustrating the

polishing process near polishing tool (3). As can be seen from Figure 17, slurry SL and electrolyte EL are fed from grooves (23b) of electrode plate (23) in the vicinity of smoothing element (24), and slurry SL and electrolyte EL pass through smoothing element (24) and are fed onto wafer W from the entire surface of smoothing element (24). Because passive film (108) formed on metal film (107) is passive to the electrolytic action of electrolyte EL, the elution of copper that forms metal film (107) into electrolyte EL can be suppressed. Consequently, little current flows through metal film (107), and the current monitored by said ammeter (62) is low and stable. Figure 25 is a graph illustrating an example of the current monitored by ammeter (62) in the electrolytic composite polishing process in the present embodiment. The aforementioned state corresponds to the condition close to the starting point of the current shown in Figure 25.

[0057]

As smoothing element (24) is rotated, the projecting portions of passive film (108), that is, passive film (108) on bumps of metal film (107) are mechanically removed by the mechanical removal action of the smoothing element or the mechanical removal action of abrasive particles PT made of, e.g., aluminum oxide, contained in slurry SL. On the other hand, as shown in Figure 18, the projecting portions of passive film (108) beneath polishing tool (3) which are present on metal film (108) [sic; (107)] are removed by the mechanical removal action of polishing tool (3), or the mechanical removal action of abrasive particles PT.

[0058]

In this way, as shown in Figure 19, passive film (108) formed on bumps of metal film (107) are selectively removed, and metal film (107) is exposed to the surface at those portions where said passive film (108) has been selectively removed.

[0059]

When metal film (107) is exposed to the surface, the exposed portions of metal film (107) as bumps are selectively eluted (process PR5). In this case, as shown in Figure 18, electrolyte EL acts to elute copper ions Cu⁺ for copper that forms metal film (107) from the bumps of metal film (107), where passive film (108) has been removed, into electrolyte EL. In this way, negative electrons e⁻ flow in metal film (107), and, as shown in Figure 17, said negative electrodes e⁻ flow from the surface of metal film (107) via electrolyte EL to electrode plate (23), forming said current i₂.

[0060]

As explained above, copper that forms metal film (107) can increase the current density as compared with passive film (108), so that it is under the concentrated electrolytic function and is selectively eluted. As a result, removal of the material is accelerated. Also, since power is fed through electrolyte EL, when there is a contact potential difference between metal film (107) as the anode and polishing tool (3) as the cathode, if the inter-electrode distance becomes shorter, that is, if the electrical resistance is reduced, the current flowing between the electrodes increases. Consequently, if there is a certain difference in the inter-electrode distance due to the bumps and dips on metal film (107) used as the anode with respect to polishing tool (3) used as the cathode (that is, for the projecting portions of metal film (107), the inter-electrode distance is shorter and the electrical resistance is lower), due to the difference in the current density, the elution rate is higher for the portion with a higher current density, as is the planarization efficiency. As shown in Figure 25, in this case, as indicated by P1, the current monitored by said ammeter (62) starts rising. Due to this function, planarization of the bump portions of metal film (107) can be carried out with greater efficiency than that when mechanical planarization is carried out.

[0061]

Due to the aforementioned function, as shown in Figure 20, the surface of metal film (107) after completion of the selective electrolyte composite polishing for perfect planarization of bumps of metal film (107) becomes a composite surface of passive film (108) left in dips of metal film (107) and the regenerated copper surface formed after removal of bumps of metal film (107).

[0062]

Then, as shown in Figure 21, for the surface of said metal film (107), electrolytic composite polishing is carried out (process PR7), which combines the mechanical polishing by means of polishing tool (3) and abrasive particles PT in slurry SL, and the electrolytic function by means of electrolyte EL. In this case, as explained above, the mechanical strength of residual passive film (108) is lower than that of the regenerated copper surface, so that when passive film (108) is subject to electrolytic composite polishing, removal takes place mainly due to mechanical action. Then, as the copper surface underlying it is exposed, the electrolytic action rises in proportion to the area of the exposed copper surface. At the time that passive film (108) is fully removed, the surface area of copper that forms metal film (107) is maximum. At the same time, the current monitored by ammeter (62) rises from time P1 shown in Figure 25 together with removal of passive film (108), and it reaches a maximum value at time P2 when

the surface area of copper is at a maximum. Because of the process up to this point, the planarization of the initial bumps and dips on the surface of metal film (107) is completed.

[0063]

In this way, in the electrolytic composite polishing operation in the present embodiment, because the polishing rate is raised with the electrochemical polishing operation, it is possible to perform polishing at a processing pressure lower than that required the conventional chemical mechanical polishing. This is highly favorable as compared with the simple mechanical polishing operation because of reduced scratching, formation of steps, dishing, erosion, etc. In addition, it is possible to perform polishing under a lower processing pressure, so that this method becomes highly favorable in the case when interlayer insulating film (102) is made of an organic type low-dielectric-contact film or porous low-dielectric-contact insulating film that has low mechanical strength and used to be prone to damage in the conventional chemical mechanical polishing operation.

[0064]

When electrolytic composite polishing of said metal film (107) is carried out so that the excess metal film (107) is removed, as shown in Figure 22, barrier film (105) is exposed (process P8). In this case, the current monitored by ammeter (62) is at a maximum at the time indicated by P2 in Figure 25 when all of passive film (108) on metal film (107) is removed, and it levels off at the time indicated by P3 in Figure 25 when barrier film (105) is exposed. When barrier film (105) is exposed, because the electrical resistance of Ta, Ti, TaN, TiN, or another material used in this case is higher than copper, the current monitored by ammeter (62) starts falling at time P3 shown in Figure 25 when the exposure of barrier film (105) starts. In this state, the polishing processing is stopped with an uneven copper metal film (107) remaining. The termination of the polishing processing of polishing apparatus (1) in this case is based on the judgment of controller (55) that the current falls below a prescribed level as indicated at P4 in Figure 25.

[0065]

Then, barrier film (105) is removed (process PR9). In the process of removal of barrier film (105), instead of slurry SL that has a high polishing rate for metal film (107) made of copper, another slurry SL that has a high polishing rate for barrier film (105) made of Ta, TaN, Ti, TiN, etc. and a low polishing rate for metal film (107) is used. That is, slurry SL with a highly selective polishing rate between barrier film (105) and metal film (107) is used in this case.

[0066]

In addition, from the standpoint of suppressing dishing and erosion due to overpolishing, removal of barrier film (105) by polishing is carried out with an output voltage from electrolysis power source (61) below that used in the aforementioned process. Also, it is preferred that the processing pressure of polishing tool (3) be lower than that in the aforementioned process. Also, since the output voltage of electrolysis power source (61) is lower and interlayer insulating film (102) is exposed to the surface after removal of barrier film (105), the magnitude of the electrolytic current is also reduced. Consequently, one may monitor the electrical resistance between smoothing element (24) and polishing tool (3) by means of said resistance meter (63), instead of monitoring the electrolytic current with said ammeter (62).

[0067]

When barrier film (105) is removed, as shown in Figure 23, interlayer insulating film (102) is exposed to the surface (process P10). When interlayer insulating film (102) is exposed, as shown in Figure 23, because the exposed portion is free of metal film (107) or barrier film (105) that acts as the anode in feeding power to the surface, power from smoothing element (24) is cut off, and the electrolytic function at the exposed portion of interlayer insulating film (102) stops. At this time, the magnitude of the electrical resistance monitored by resistance meter (63) begins to increase.

[0068]

As in the aforementioned case when the bumps of metal film (107) are reduced, the same process takes place between the residual portion of metal film (107) and the exposed portion of barrier film (105). That is, with barrier film (105) used as the portion with the higher electrical resistance in place of passive film (108), the current density becomes concentrated at the residual portion of metal film (107), so that the residual portion of metal film (107) is eluted and removed. For the portion where the electrolytic function stops, the main function becomes the mechanical removal function of material due to polishing tool (3) and slurry SL.

[0069]

However, in the conventional chemical mechanical polishing operation, the selectivity of polishing rate is chosen to be as high as possible for barrier film (105) and metal film (107) with respect to interlayer insulating film (102), and with the difference in the polishing rate used as a margin, the dimensional precision of the upper surface of interlayer insulating film (102) is guaranteed. Consequently, with this constitution, dishing of metal film (107) becomes inevitable. On the other hand, if the selectivity is chosen to be low, although dishing can be alleviated to a

certain extent, removal of barrier film (105) and metal film (107) may be insufficient because the dimensional precision depends on the uniformity of the distribution of the removal rate within the wafer surface. Consequently, in order to prevent underpolishing in a state with residual barrier film (105) and metal film (107) left on the upper surface of interlayer insulating film (102), it is necessary to perform overpolishing corresponding to the extent of nonuniformity of the removal rate on the surface, and degradation in erosion due to this overpolishing operation also becomes essentially inevitable. On the other hand, in the present embodiment, if the uniformity on the surface of wafer W is guaranteed to a certain extent, residual barrier film (105) or residual portion of metal film (107) left on interlayer insulating film (102) can be removed with great efficiency due to the electrolytic function, and elution from the exposed portion of interlayer insulating film (102) stops. Consequently, it is possible to guarantee the dimensional precision of interlayer insulating film (102) automatically, and to suppress generation of dishing and erosion.

[0070]

As explained above, it is possible to fully remove barrier film (105) made of, e.g., Ta, TaN, Ti, TiN, etc., and at the same time, to suppress the generation of dishing or erosion caused by overpolishing. Also, in the aforementioned process of removal of barrier film (105), if the absolute value of the current is selected to be low, and the mechanical load is also set to be low, the removal rate is reduced. However, if metal film (107) of copper in the remaining portion where the residual film thickness is uneven, the removal amount of barrier film (105) will itself be small since barrier film (105) is thinner than metal film (107), and in this process, even when there is variation or unevenness, the absolute values of dishing and erosion still can be reduced to a negligible level, and the processing time also can be shortened. In addition, in the polishing method pertaining to the present embodiment, a composite processing is carried out made up of both mechanical and electrochemical components. Consequently, it is possible to produce a planarized surface with little damage and a high degree of mechanical planarization.

[0071]

Then, based on the electrical resistance monitored by resistance meter (63), at the time when the electrical resistance is maximum, that is, at the end of wiring formation, the process of removal of barrier film (105) comes to an end (process PR11). Controller (55) determines the value of electrical resistance, and stops the processing operation of polishing apparatus (1). Also, before the end of the polishing process, while the electrolytic function is applied, polishing tool (3) is driven to move without making contact with the surface of wafer W, for example, at a height of about 100 μm above the surface of the wafer. In this way, it is possible to form a

damage-free surface by means of only the electrolytic function, without performing mechanical polishing. In this way, as shown in Figure 23, wiring (109) and contact [holes] (110) are finally formed in interlayer insulating film (102).

[0072]

Then, the semiconductor device with wiring (109) and contact (110) formed thereon is rinsed (process PR12). In this rinsing process, immediately after the formation of wiring (109) and contact (110), a cleaning chemical solution and an oxidation inhibitor are fed onto the surface of wafer W, with no power applied to wafer W. As shown in Figure 24, a positive pulsed voltage is applied to polishing tool (3), and washing is performed by means of pure water and chemical solution, so as to remove slurry SL and particles present on the surface of wafer W. In the present embodiment, before rinsing, because abrasive particles PT made of alumina and contained in slurry SL are positively charged so as to improve the dispersion property of the abrasive particles, even when the abrasive particles are left without attrition after they are made to mechanically collide on the surface of metal film (107) made of copper, they still do not become embedded in the surface of copper that forms metal film (107) as the anode. As shown in Figure 23, they re-attach to on the surface of polishing tool (3) and are used in the next processing cycle. In addition, because the positively charged particles are attracted to the surface of polishing tool (3) as the anode, they do not become embedded in the surface of copper. On the other hand, the negatively charged particles left on the surface of wafer W also can be removed from the surface of wafer W by means of the aforementioned rinsing operation. Also, even if a slurry SL with abrasive particles PT with a negative charge is used, it also can be removed. When copper is used as the wiring forming material, it tends toward oxidation, and it is necessary to remove the metal ions and particles without modification of the copper surface. In the present embodiment, this problem is solved since abrasive particles PT are pre-charged positively, and rinsing is carried out. Also, in the aforementioned example, aluminum oxide (alumina) is used. However, it is also possible to use cerium oxide, silica, germanium oxide, etc., with the same results.

[0073]

As explained above, in the semiconductor device manufacturing method of the present embodiment, passive film (108) is formed on metal film (107) that buries the wiring groove wiring [sic; wiring grooves] and contact holes formed in insulating film (102); passive film (108) formed on bumps of metal film (107) is selectively removed; with the residual passive film (108) used as a mask, metal film (107) exposed to the surface is selectively removed by means of electrolytic polishing since the current density increases for removal. In this way, the initial

bumps and dips can be planarized at a much higher efficiency than that in the conventional CMP. Also, for metal film (107) that has the initial bumps and dips planarized, removal is performed by means of electrolytic composite polishing, a combination of electrolytic polishing and chemical mechanical polishing, so that excess metal film (107) can be removed with a much greater efficiency than that of conventional CMP. Consequently, even when the processing pressure of polishing tool (3) is reduced, a sufficient polishing rate can still be obtained, and damage to metal film (107) can be reduced. At the same time, dishing and erosion can be suppressed.

[0074]

In the semiconductor device manufacturing method of the present embodiment, at the time that excess metal film (107) is removed and barrier film (105) is exposed, polishing is stopped, and slurry SL is changed to a type with a higher polishing rate for barrier film (105). Also, the output voltage of electrolysis power source (61) and other polishing conditions are changed to remove excess barrier film (105). As a result, even when overpolishing is required for removal of excess barrier film (105), it is still possible to suppress dishing and erosion to low levels.

[0075]

Also, in the semiconductor device manufacturing method of the present embodiment, because polishing of the metal film is carried out by means of electrolytic composite polishing with high efficiency, one can reduce the processing pressure of polishing tool (3). Consequently, even when the dielectric contact is reduced from the standpoint of lower power consumption and higher processing speed by using an organic type low-dielectric-contact film or porous low-dielectric-contact film having a relatively low mechanical strength as interlayer insulating film (102), it is still possible to alleviate damage to such insulating films.

[0076]

In the aforementioned embodiment, it is possible to control the absolute value of the polishing processing amount of the metal film by controlling the integration of the electrolytic current and the time for polishing tool (3) to pass above wafer W. In the aforementioned embodiment, the process of copper wiring formation was presented as an example. However, the present invention is not limited to this example. It is also possible to adopt the present invention in the process of formation of metal wiring made of tungsten, aluminum, silver, etc.

[0077]

In the aforementioned embodiment, the case of electrolytic composite polishing as a combination of chemical mechanical polishing using slurry SL and electrolytic polishing using electrolyte EL was explained. However, the present invention is not limited to this example. For instance, the present invention also allows the omission of slurry SL, and electrolytic composite polishing is carried out as a combination of electrolytic polishing using electrolyte EL and mechanical polishing using polishing surface (3a) of polishing tool (3).

[0078]

Also, in the aforementioned embodiment, the current flowing between polishing tool (3) and electrode plate (23) is monitored, and based on this value, the polishing process is controlled until barrier film (105) is exposed. However, it is also possible to monitor the entire polishing process. Similarly, in the aforementioned embodiment, the electrical resistance between polishing tool (3) and electrode plate (23) is monitored, and based on this value, the process of removal of only barrier film (105) is controlled. However, it is also possible to control the entire polishing process by means of the monitored electrical resistance.

[0079]

Embodiment Variant 1

Figure 26 is a schematic diagram illustrating an embodiment variant of the polishing apparatus of the present invention. In polishing apparatus (1) in the aforementioned embodiment, the supply of power to the surface of wafer W is carried out by means of an electroconductive polishing tool and conducting plate (23) having smoothing element (24). In the system shown in Figure 26, wheel-shaped polishing tool (401) is also electroconductive, like polishing apparatus (1), as is wafer table (402) to which wafer W is chucked for rotation. Power is supplied to polishing tool (401) under the same conditions as in the aforementioned embodiment. In this case, to feed power to wafer table (402), rotary joint (403) is set in the lower portion of wafer table (402), so that the supply of power is always maintained to rotating wafer table (402) by means of rotary joint (403). In this constitution, electrolytic current is sourced.

[0080]

Embodiment Variant 2

Figure 27 is a schematic diagram illustrating another embodiment variant of the polishing apparatus of the present invention. In this example, wafer table (502) to which wafer W is chucked is rotated, and wafer W is supported by retaining ring (504) arranged on the periphery of wafer W. Not only polishing tool (501) but also retaining ring (504) is made

electroconductive, and power is fed to polishing tool (501) under the same conditions as in the aforementioned embodiment. Also, retaining ring (504) covers up to the aforementioned barrier layer portion formed on wafer W for supplying power. In addition, power is fed through rotary joint (503) arranged in the lower portion of wafer table (502) to retaining ring (504). Also, even when polishing tool (501) makes contact with wafer W, since the degree of inclination of polishing tool (3) is increased such that a gap greater than the thickness of retaining ring (504) can be maintained in the edge portion, it is possible to prevent interference between polishing tool (501) and retaining ring (504).

[0081]

Embodiment Variant 3

Figure 28 is a schematic diagram illustrating yet another embodiment of the polishing apparatus of the present invention. For the polishing apparatus shown in Figure 28, the electrolytic polishing function of the present invention is added to a conventional CMP apparatus. In this polishing apparatus, the entire surface of wafer W chucked by wafer chucks (207) is rotated and brought in contact with the polishing surface of the polishing tool prepared by bonding polishing pad (polishing cloth) (202) to fixed disk (201), so that the surface of wafer W is planarized. On polishing pad (202), anode electrodes (204) and cathode electrodes (203) are arranged alternately in a radial configuration. Also, anode electrodes (204) and cathode electrodes (203) are electrically insulated from each other by means of insulator (206). Power is fed from the side of fixed disk (201) to anode electrodes (204) and cathode electrodes (203). The aforementioned anode electrodes (204) and cathode electrodes (203) as well as insulator (206) form polishing pad (202). Also, wafer chucks (207) are made of an insulating material. In addition, in this polishing apparatus, there is feeding unit (208) for feeding electrolyte EL and slurry SL to the surface of polishing pad (202), so as to enable electrolytic composite polishing as a combination of electrolytic polishing and chemical mechanical polishing.

[0082]

Figure 29 is a diagram illustrating the electrolytic composite polishing operation in the polishing apparatus with the aforementioned constitution. Also, copper film (210) is formed on the surface of wafer W. As shown in Figure 29, during the process of electrolytic composite polishing, electrolyte EL and slurry SL are included between copper film (210) formed on the surface of wafer W and the polishing surface of polishing pad (202), while a DC voltage is applied between anode electrode (204) and cathode electrode (203), so that current i flows from anode electrode (204) through electrolyte EL, copper film (210), and then electrolyte EL again to reach cathode electrode (203). In this case, in the vicinity inside circle G shown in Figure 29, due

to the electrolytic function, copper film (210) is eluted, and at the same time, copper film (210) is removed under the mechanical removal function of polishing pad (202) and slurry SL.

[0083]

With the aforementioned constitution, the same effect as that of polishing apparatus (1) in the aforementioned embodiment can be realized. Also, the configuration of anode electrodes and cathode electrodes formed on the polishing pad is not limited to the constitution shown in Figure 28. For example, the configuration shown in Figure 30 may also be adopted. In this configuration, multiple linear shaped anode electrodes (222) are arranged in a checkerboard configuration at an equal distance from each other, and cathode electrodes (223) are arranged in the various rectangular regions defined by said anode electrodes (222). Polishing pad (221) is formed from anode electrodes (222) and cathode electrodes (223) electrically insulated from each other by insulator (224). In addition, the configuration shown in Figure 31 may be adopted. In this configuration, annular anode electrodes (242) having different radii are arranged concentrically, and cathode electrodes (243) are set in the annular regions formed between said anode electrodes (242). Polishing pad (241) is formed from anode electrodes (242) and cathode electrodes (243) electrically insulated from each other with insulator (244).

[0084]

Effect of the invention

According to the present invention, the metal film is polished under the composite effect of mechanical polishing and electrolytic polishing. Consequently, compared with the case of the planarization of the metal film using mechanical polishing, bumps of the metal film can be selectively removed and planarized with much greater efficiency. Also, according to the present invention, power is supplied with the polishing tool used as the cathode. Consequently, the particles and abrasive particles in the polishing agent that are positively charged beforehand are attracted to the polishing tool, so that it is possible to prevent them from remaining on the wafer surface, and the efficiency can thereby be increased. Also, according to the present invention, since the metal film can be removed with great efficiency, a sufficiently high polishing rate can be realized with a relatively low polishing pressure. Consequently, it is possible to suppress the occurrence of scratching, dishing, erosion, etc. on the polished metal film. In addition, according to the present invention, a sufficiently high polishing rate can be obtained at relatively low polishing pressure. Consequently, even when the dielectric contact is reduced from the standpoint of lower power consumption and higher processing speed by using an organic type low-dielectric-contact film or porous low-dielectric-contact film having a relatively low mechanical strength as the interlayer insulating film, it is still possible to perform the operation

rather easily. Also, according to the present invention, the residual barrier film left on the interlayer insulating film or the metal portion is removed by the electrolytic action with great efficiency, and elution from the exposed portion of the insulating film is stopped. Consequently, it is possible to guarantee the stopping of polishing automatically with high precision, and it is possible to suppress dishing or erosion. In addition, according to the present invention, by monitoring the electrolytic current, one can control the polishing process and correctly monitor the progress of the polishing process. Moreover, according to the present invention, by monitoring the electrical resistance between the polishing tool and the electrode member, one can correctly control the polishing process even when polishing a film, where the current flow is low or nonexistent, together with the metal film.

Brief description of the figures

Figure 1 is a diagram illustrating the configuration of an embodiment of the polishing device disclosed in the present invention.

Figure 2 is an enlarged view illustrating the details of the head part of the polishing device shown in Figure 1.

Figure 3(a) is a bottom view illustrating an example of the structure of electrode plate (23). Figure 3(b) is a cross-sectional view illustrating the position relationship among electrode plate (23), electroconductive shaft (20), scrubbing part (24), and insulating part (4).

Figure 4 is a diagram illustrating the relationship between a polishing tool and a wafer.

Figure 5 is a diagram illustrating the movement of the wafer in the direction of the X axis with respect to the polishing tool.

Figure 6 is a schematic diagram illustrating the polishing the wafer with the head processing part.

Figure 7 is a diagram illustrating the relationship between a polishing tool and an electrode plate.

Figure 8 is a diagram explaining the electrolytic polishing function of the polishing device disclosed in the present invention.

Figure 9 is a flow chart illustrating the manufacturing process in an embodiment of the semiconductor device manufacturing method disclosed in the present invention.

Figure 10 is a cross-sectional view illustrating the manufacturing process of the semiconductor device manufacturing method disclosed in the present invention.

Figure 11 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 10.

Figure 12 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 11.

Figure 13 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 12.

Figure 14 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 13.

Figure 15 is an enlarged view illustrating the cross-sectional structure of the semiconductor device shown in Figure 14.

Figure 16 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 14.

Figure 17 is a conceptual diagram illustrating the polishing process near scrubbing part (24).

Figure 18 is a conceptual diagram illustrating the polishing process near polishing tool (3).

Figure 19 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 16.

Figure 20 is a cross-sectional view illustrating the state after projections of the metal film are selectively removed and planarized.

Figure 21 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 19.

Figure 22 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 21.

Figure 23 is a cross-sectional view illustrating the manufacturing process after the step shown in Figure 22.

Figure 24 is a cross-sectional view illustrating the state after flashing is performed with respect to the polished semiconductor device.

Figure 25 is a diagram illustrating an example of the monitored current value during the composite electrolytic polishing process.

Figure 26 is a diagram illustrating a embodiment variant of the polishing device disclosed in the present invention.

Figure 27 is a diagram illustrating yet another embodiment variant of the polishing device disclosed in the present invention.

Figure 28 is a schematic diagram illustrating another embodiment of the polishing device disclosed in the present invention.

Figure 29 is a diagram explaining the composite electrolytic polishing operation carried out by the polishing device shown in Figure 28.

Figure 30 is a diagram illustrating another example of the electrode configuration of the polishing pad.

Figure 31 is a diagram illustrating yet another example of the electrode configuration of the polishing pad.

Figure 32 is a cross-sectional view illustrating the wiring forming process carried out using the dual damascene method.

Figure 33 is a cross-sectional view illustrating the wiring forming process carried out after the step shown in Figure 32.

Figure 34 is a cross-sectional view illustrating the wiring forming process carried out after the step shown in Figure 33.

Figure 35 is a cross-sectional view illustrating the wiring forming process carried out after the step shown in Figure 34.

Figure 36 is a cross-sectional view illustrating the wiring forming process carried out after the step shown in Figure 35.

Figure 37 is a cross-sectional view illustrating the wiring forming process carried out after the step shown in Figure 36.

Figure 38 is a cross-sectional view explaining dishing of a metal film during polishing processing carried out with the CMP method.

Figure 39 is a cross-sectional view explaining erosion of a metal film during polishing processing carried out with the CMP method.

Figure 40 is a cross-sectional view explaining recess formation on a metal film during polishing processing carried out with the CMP method.

Figure 41 [text missing in the original] occurring on a metal film during polishing processing carried out with the CMP method.

Brief description of the reference numbers

- 1 Polishing device
- 11 Processing head part
- 61 Electrolytic power supply
- 55 Controller
- 55, 71 Slurry supply devices
- 81 Electrolyte supply device

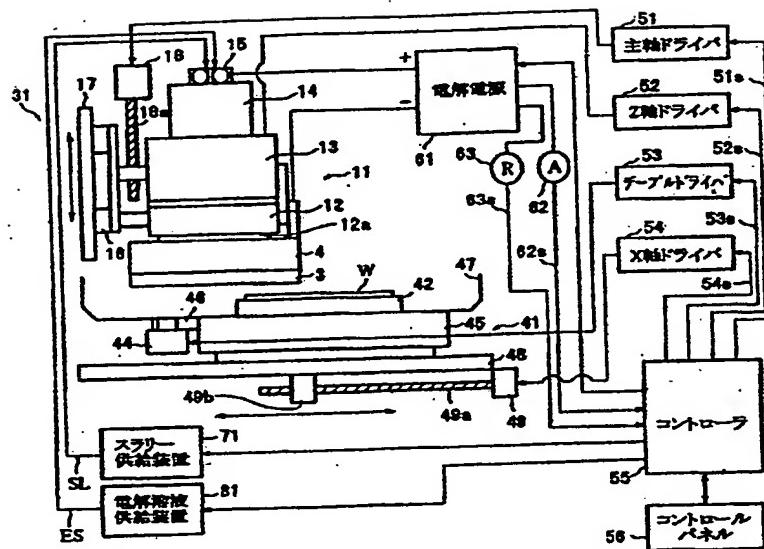


Figure 1

- Key:
- 51 Main axis driver
 - 52 Z-axis driver
 - 53 Table driver
 - 54 X-axis driver
 - 55 Controller
 - 56 Control panel
 - 61 Electrolytic power supply
 - 71 Slurry supply device
 - 81 Electrolyte supply device

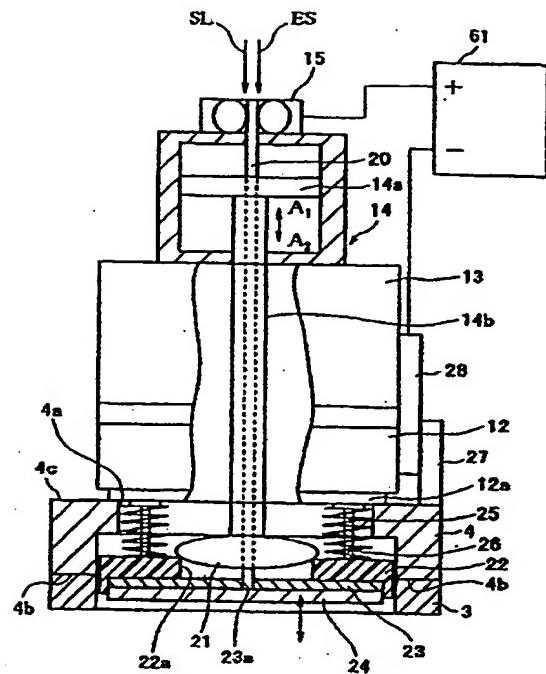


Figure 2

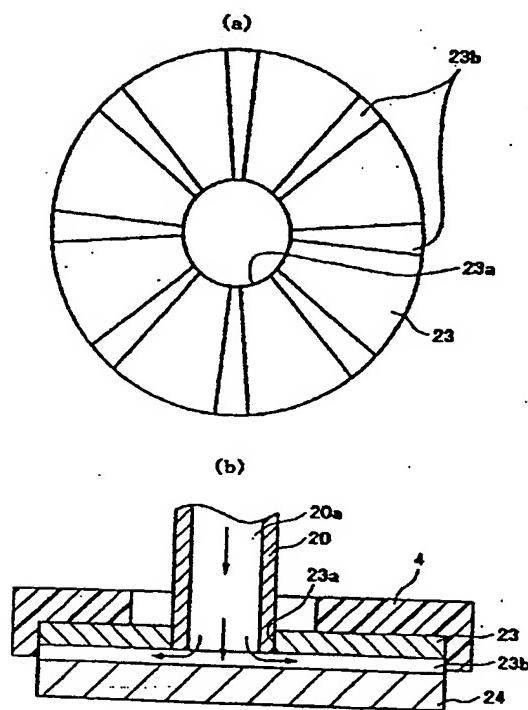


Figure 3

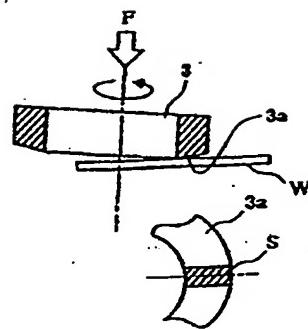


Figure 4

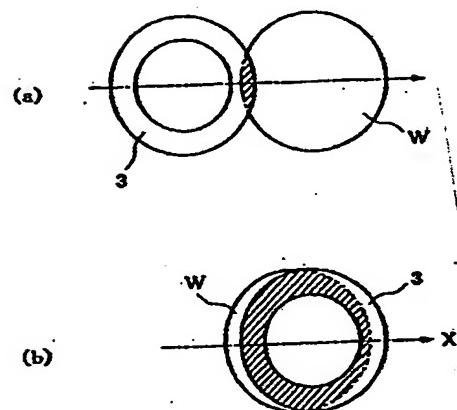


Figure 5

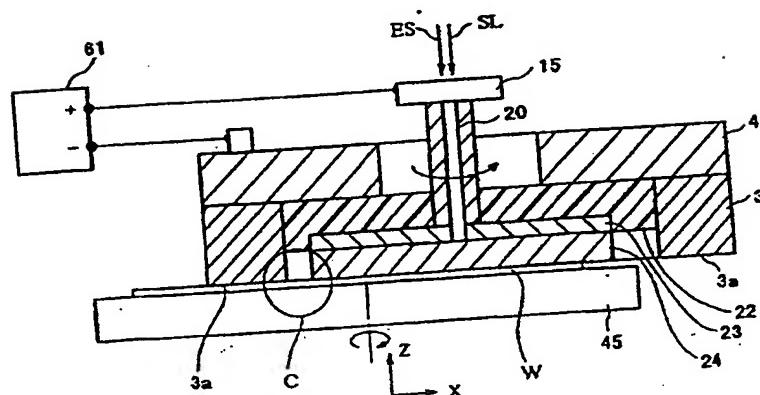


Figure 6

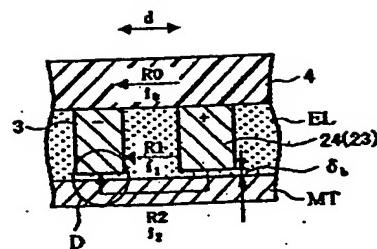


Figure 7

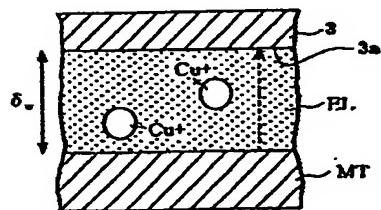


Figure 8

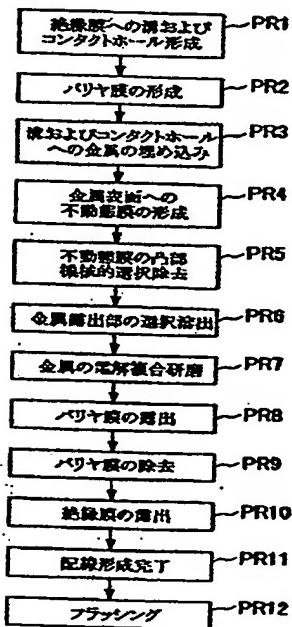


Figure 9

- Key:
- PR1 Form grooves and contact holes on insulating film
 - PR2 Form barrier film
 - PR3 Bury metal in the grooves and contact holes

- PR4 Form passive film on the metal surface
- PR5 Selectively remove projections of the passive film by means of mechanical polishing
- PR6 Selectively elute metal projections
- PR7 Composite electrolytic polishing of the metal
- PR8 Expose barrier film
- PR9 Remove barrier film
- PR10 Expose insulating film
- PR11 Complete formation of wiring
- PR12 Rinsing

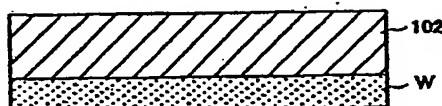


Figure 10

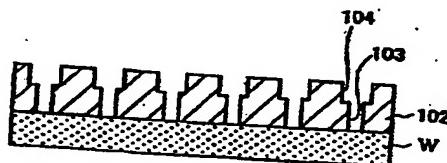


Figure 11

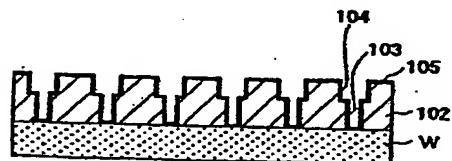


Figure 12

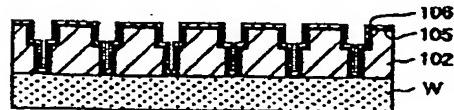


Figure 13

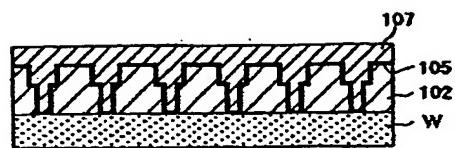


Figure 14

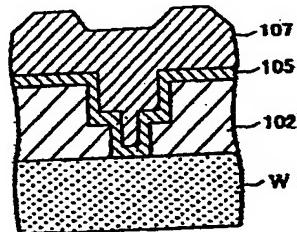


Figure 15

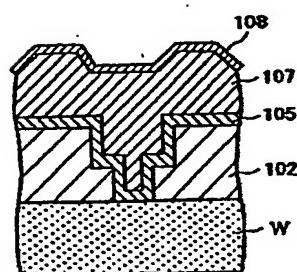


Figure 16

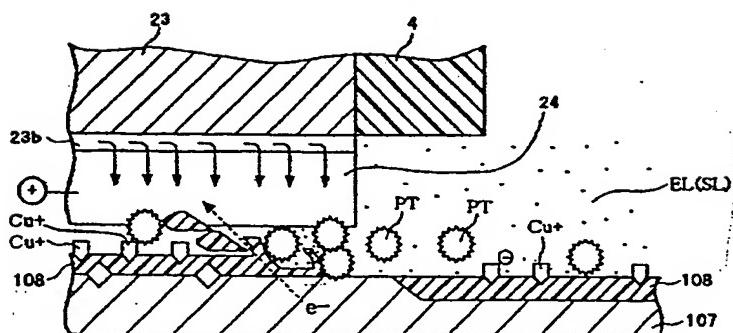


Figure 17

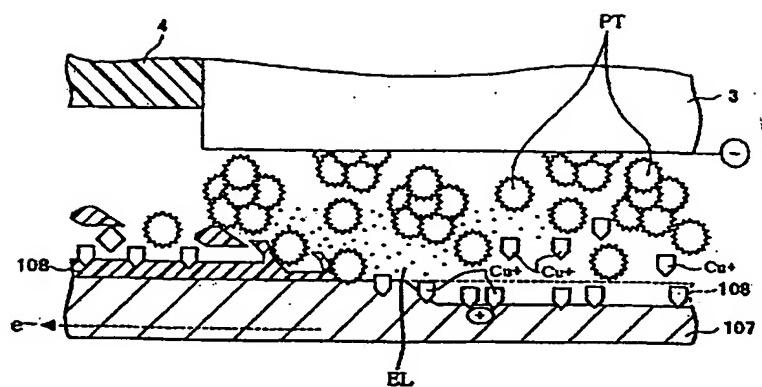


Figure 18

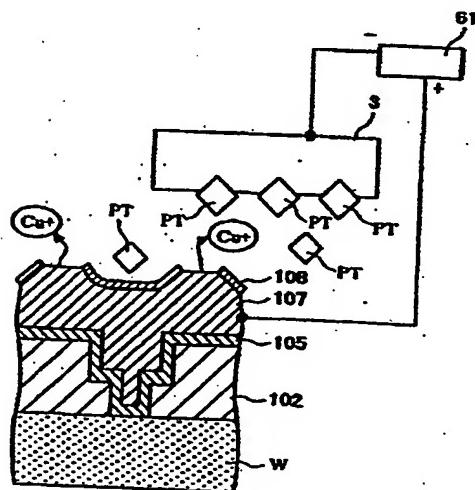


Figure 19

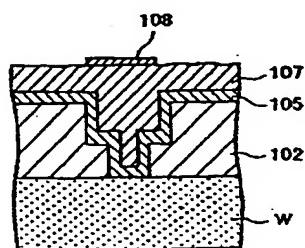


Figure 20

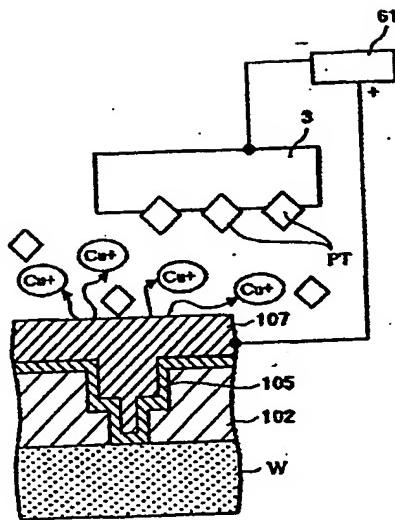


Figure 21

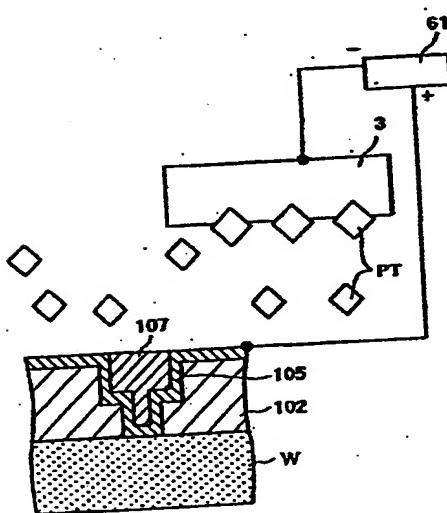


Figure 22

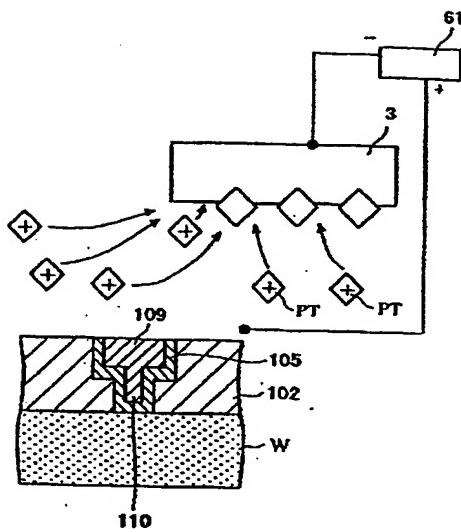


Figure 23

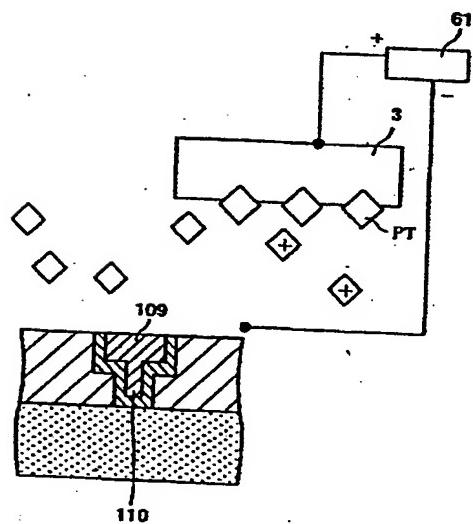


Figure 24

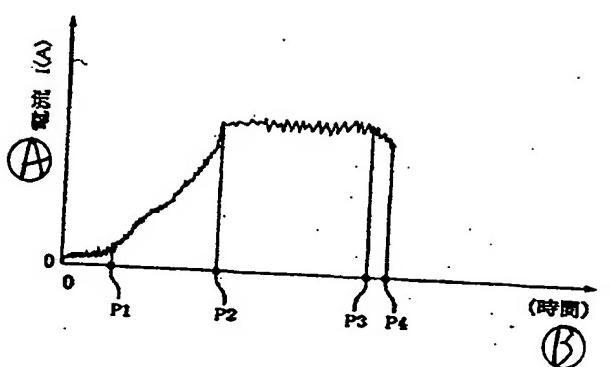


Figure 25

Key: A Current (A)
B Time

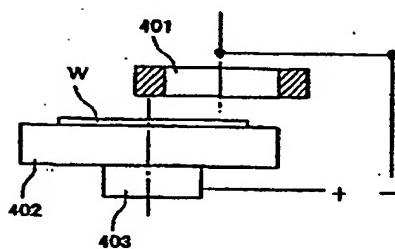


Figure 26

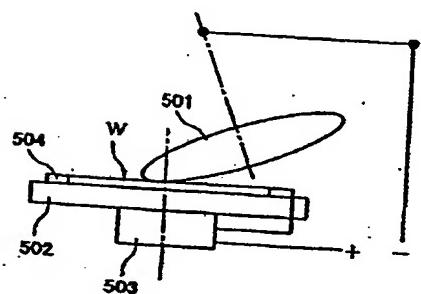


Figure 27

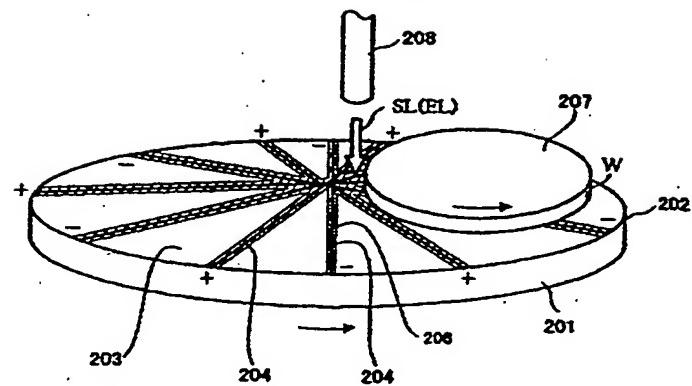


Figure 28

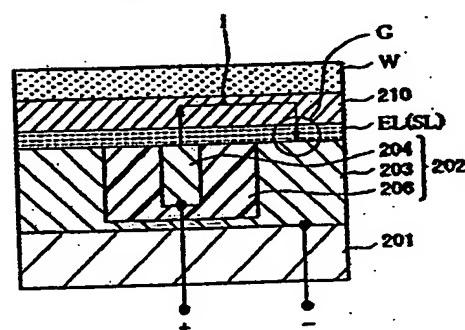


Figure 29

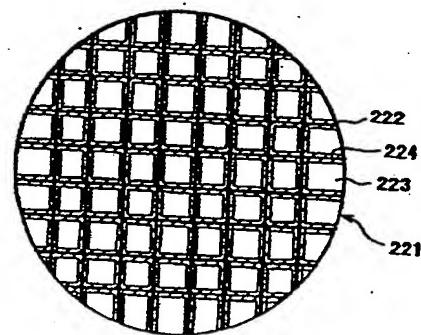


Figure 30

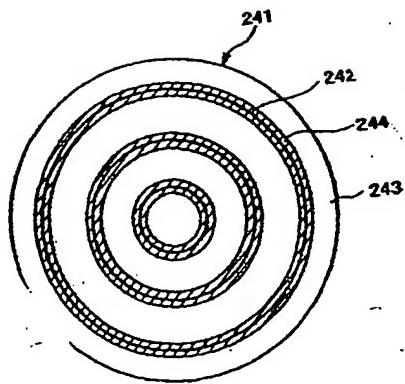


Figure 31

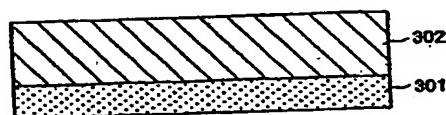


Figure 32

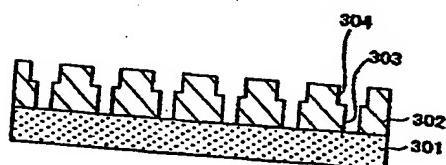


Figure 33



Figure 34

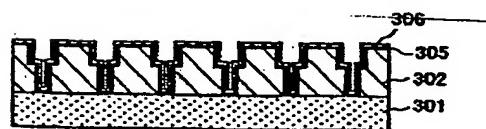


Figure 35

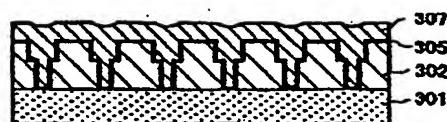


Figure 36

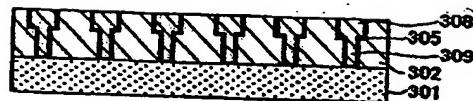


Figure 37

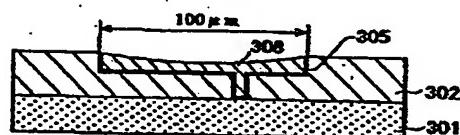


Figure 38

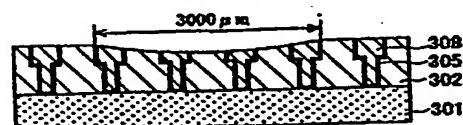


Figure 39

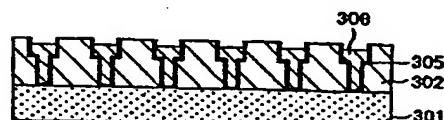


Figure 40

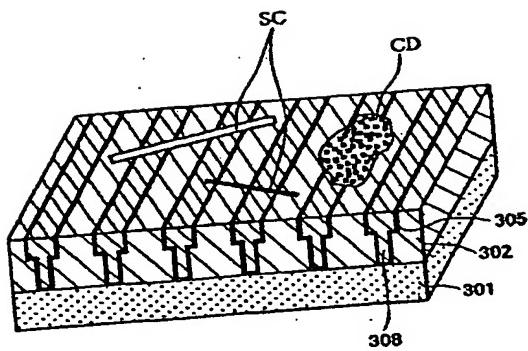


Figure 41